Workstation Hardware

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The [illegible] pages update [illegible] Edition A-09-00016-01-A and Update Notices A-09-[illegible]-01-A, A-09-00066-01-A, and A-09-[illegible]-01-A or [illegible] A-09-00016-[illegible] and Update Notices A-09-00066-01-A and A-09-[illegible] of the Workstation Hardware Manual

Insert these pages according to the collating instructions on the back of this Notice

Updated pages are indicated by a date at the bottom of the page

Throughout the Manual, change bars in the margins indicate technical additions and changes. Asterisks indicate deletions. Editorial changes are [illegible] changes will be incorporated into the next edition of this Manual

Insert this page after the title page of your Manual to provide a record of the update

Convergent Technologies

COLLATING INSTRUCTIONS

The Workstation Hardware Manual has been divided into two volumes.

A second binder, new front matter (Tables of Contents, etc.) as well as new tab dividers and spine inserts are included with this Update Notice.

VOLUME 1: Sections 1 - 9

Delete	Replace with
- - - - - - - -	Volume 1 Title Page
i to xvi	iii to xxii
2-25, 2-26	2-25, 2-26
4-47 to 4-50	4-47 to 4-50
5-1	5-1
5-3 to 5-8	5-3 to 5-8

Place the 7 foldout pages (schematic) of the 64K I/O-Memory board at the end of Section 5. (Do not delete the existing schematic.)

VOLUME 2: Sections 10 - 14
Glossary
Appendixes A - G

Delete		Replace with
- - - - - - - -		Volume 2 Title Page
- - - - - - - -		iii to v
- - - - - - - -		14-1
D-1 to D-4	(Appendix C)	D-1 to D-4
- - - - - - - -	(Appendix D)	E-1
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- - - - - - - -	(Appendix F)	G-i to G-50
- - - - - - - -	(Appendix G)	H-1 to H-93

DESCRIPTION OF CHANGES

Revisions to include information on the 64K I/O-Memory board have been made in Sections 2, 4, and 5 and in Appendix C. A new schematic has been added to Section 5.

Appendix F descibes the IWS Graphics Control board.

Appendix G contains revised schematics to update previous versions appearing throughout this manual. (Do not delete existing schematics.)

Workstation Hardware

Volume 1

Convergent Technologies

Convergent Technologies

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WORKSTATION HARDWARE MANUAL

Volume 1

First Edition Revised (April 1981) A-09-00016-01-B

CONTENTS: Volume 1

9. Keyboard

LIST OF FIGURES

This Manual is one of a set that documents the Convergent™ Family of Information Processing Systems. The set can be grouped as follows:

Introductory
- Installation Guide
- Operator's Guide
- Executive Manual

Hardware
- Workstation Hardware Manual
- Peripherals Hardware Manual
- AWS-210 Hardware Manual
- AWS-220, -230, -240 Hardware Manual

Operating System
- CTOS™ Operating System Manual
- System Programmer's Guide
- System Utilities Manual
- Batch Manual

Programming Languages
- COBOL Manual
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- BASIC Manual
- BASIC Compiler Manual
- Pascal Manual
- Assembly Language Manual

Program Development Tools
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- Debugger Manual
- Linker/Librarian Manual

Data Management Facilities
- ISAM Manual
- Forms Manual
- Sort/Merge Manual

Text Management Facilities
- Word Processing User's Guide
- Word Processing Reference Manual
- Word Processing Quick Reference

Applications Facilities
- Multiplan
- Business Graphics User's Guide
- Business Graphics Reference Manual
- Graphics Programmer's Guide
- Font Designer Manual

Communications

- Asynchronous Terminal Emulator Manual
- 3270 Terminal Emulator Manual
- 2780/3780 RJE Terminal Emulator Manual
- SNA Network Gateway Manual
- SNA 3270 Emulator Manual
- X.25 Network Gateway Manual
- Multimode Terminal Emulator User's Guide
- Multimode Terminal Emulator Reference Manual

This section outlines the contents of these manuals.

Introductory

The Installation Guide describes the procedure for unpacking, cabling, and powering up a system.

The Operator's Guide addresses the needs of the average user for operating instructions. It describes the workstation switches and controls, keyboard function, and floppy disk handling.

The Executive Manual describes the command interpreter, the program that first interacts with the user when the system is turned on. It specifies commands for managing files and invoking other programs such as the Editor and the programming language compilers.

Hardware

The Workstation Hardware Manual describes the mainframe, keyboard, and video display for the IWS family of workstations. It specifies system architecture, printed circuit boards (Motherboard, Processor, I/O-Memory, Video Control, Graphics Control Board, ROM and RAM Expansions), keyboard, video monitor, Multibus interface, communications interfaces, power supply, and environmental characteristics of the workstation.

The Peripherals Hardware Manual describes the disk subsystems. It specifies the disk controller Motherboard, controller boards for the floppy disk and the Winchester disks, power supplies, disk drives, and environmental characteristics.

The AWS-210 Hardware Manual describes the mainframe, keyboard, and video display of the AWS-210 workstation. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, and CPU), keyboard, video monitor, expansion interface, cluster communications interface, power supply, and environmental characteristics of the workstation.

The AWS-220, -230, -240 Hardware Manual describes the mainframe, keyboard, disk controllers, and video display of the AWS-220, -230, and -240 workstations. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, 8088 CPU, 8086 CPU, Floppy Disk Controller, and Hard Disk Controller), keyboard, video monitor, cluster communications interface, external interfaces, power supply, and environmental characteristics of the workstation.

Operating System

The CTOS™ Operating System Manual describes the Operating System. It specifies services for managing processes, messages, memory, exchanges, tasks, video, disk, keyboard, printer, timer, communications, and files. In particular, it specifies the standard file access methods: SAM, the sequential access method; RSAM, the record sequential access method; and DAM, the direct access method.

The System Programmer's Guide addresses the needs of the system programmer or system manager for detailed information on Operating System structure and system operation. It describes (1) cluster architecture and operation, (2) procedures for building a customized Operating System, and (3) diagnostics.

The System Utilities Manual describes utilities such as Backup Volume, IVolume, Restore, Change Volume Name, PLog, Maintain File, Dump.

The Batch Manual describes the batch manager, which executes batch jobs under control of job control language (JCL) files.

Programming Languages

The COBOL, FORTRAN, BASIC [Interpreter], BASIC Compiler, PASCAL, and Assembly Language Manuals describe the system's programming languages. Each manual specifies both the language itself and also operating instructions for that language.

The Pascal Manual is supplemented by a popular text, Pascal User Manual and Report.

The Assembly Language Manual is supplemented by a text, the Central Processing Unit, which describes the main processor, the 8086. It specifies the machine architecture, instruction set, and programming at the symbolic instruction level.

Program Development Tools

The Editor Manual describes the text editor.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. Together with appropriate interlistings, it can be used for debugging FORTRAN, Pascal, and assembly language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

The Linker/Librarian Manual describes the Linker, which links together separately compiled object files, and the Librarian, which builds and manages libraries of object modules.

Data Management Facilities

The ISAM Manual describes the multikey indexed sequential access method. It specifies the procedural interfaces and shows how these interfaces are called from the various languages.

The Forms Manual describes the Forms facility that includes (1) the Forms Editor, which is used to interactively design and edit forms, and (2) the Forms run time, which is called from an application program to display forms and accept user input.

The Sort/Merge Manual describes (1) the Sort and Merge utilities that run as a subsystem invoked at the Executive command level, and (2) the Sort/Merge object modules that can be called from an application program.

Text Management Facilities

The Word Processing User's Guide introduces the Word Processor to the first-time user. It provides step-by-step lessons that describe basic word processing operations. The lessons show how to execute operations and apply them to sample text.

The Word Processing Reference Manual is a reference tool for users already familiar with the Word Processor. It describes the Word Processor keyboard and screen; basic, advanced, and programmer-specific operations; list processing; printer and print wheel configurations; and hardware considerations.

The Word Processing Quick Reference provides a concise summary of all word processing operations and briefly describes the keyboard and commands.

Applications Facilities

Multiplan is a financial modeling package designed for business planning, analysis, budgeting, and forecasting.

The Business Graphics User's Guide introduces Business Graphics to the first-time user. It provides step-by-step lessons that describe basic Business Graphics operations. The lessons show how to execute operations and apply them to sample charts.

The Business Graphics Reference Manual is a reference tool for users already familiar with Business Graphics. It describes the Business Graphics keyboard and screen; box and arrow cursor movement; obtaining information from Multiplan; operations; and plotter configurations.

The Graphics Programmer's Guide is a reference for applications and systems programmers. It describes the graphics library procedures that

can be called from application systems to generate graphic representations of data, and it includes a section on accessing Business Graphics from an application system.

The Font Designer Manual describes the interactive utility for designing new fonts (character sets) for the video display.

Communications

The Asynchronous Terminal Emulator Manual describes the asynchronous terminal emulator.

The 3270 Terminal Emulator Manual describes the 3270 emulator package.

The 2780/3780 RJE Terminal Emulator Manual describes the 2780/3780 emulator package.

The SNA Network Gateway Manual describes the SNA Network Gateway, which supports data communications over an SNA network. The SNA Network Gateway comprises the Transport Service and Status Monitor. The Transport Service allows a Convergent workstation to function as cluster controller and forms the foundation for Convergent SNA products.

The SNA 3270 Emulator Manual describes the SNA 3270 emulator package. The SNA 3270 emulator provides CRT and printer subsystems in addition to a Virtual Terminal Interface for use in application programs.

The X.25 Network Gateway Manual describes the X.25 Network Gateway, which supports CCITT Recommendation X.25 communications over a public data network. There are three levels of access to the network: packet, X.25 sequential access method, and the Multimode Terminal Emulator X.25 communications option.

The Multimode Terminal Emulator User's Guide introduces the Multimode Terminal Emulator to the first-time user. It describes the MTE video display, keyboard, display memory, and advanced operations for the X.25 communications option.

The Multimode Terminal Emulator Reference Manual is a reference tool for sophisticated users of the Multimode Terminal Emulator. It describes the MTE escape sequences and field verification program.

PREFACE

INTENDED AUDIENCE

The Workstation Hardware Manual deals with the mainframe (processing, memory and I/O-control portions of the system), the keyboard and the video subsystem for a workstation configuration of the system. The Peripherals Hardware Manual deals with the mass storage (floppy disk and Winchester disk) portions of the system.

The manual is intended for OEM engineers who will test or service the system electronics. It is not, however, intended as documentation of production-level testing nor is it designed to support modifications of the hardware. Convergent Technologies does not support modifications to its boards other than those predetermined by design, such as jumper options; the only provision for user additions to the system are through the Multibus* interface slots on the mainframe and through the conventional serial and parallel I/O connectors on the mainframe.

SOFTWARE CONTENT

The system contains several programmable peripheral ICs and registers. All of these are either initialized to default conditions by the standard operating system during power-up/Reset and/or they are supported with preprogrammed routines in the system library that can be bound to user's application programs. In addition, the operating system's interrupt service processes often reinitialize or modify the operation of this circuitry.

The descriptions given under the "Software Interface" sections of certain chapters document the interface between these software events and the hardware. With this exception, the manual concentrates exclusively on hardware.

CONVENTIONS

All numbering of bits in a word, bits on a bus line and I/O-port addresses is done in hexidecimal notation, with decimal equivalents included in parentheses for reference to CT software manuals. For example, the 20 bits in an address are numbered from 0, the least significant bit, to 13 (19 decimal), most significant bit; the signal lines on 16-bit data buses are numbered from 0 to F (0 to 15, decimal).

Signal names use plus (+) and minus (-) suffixes to distinguish active-high from active-low, respectively. For example,

Signal Name	Logical State	Voltage Level
RD-	0 (active)	Low
	1 (inactive)	High
RD+	0 (inactive)	Low
	1 (active)	High

* Multibus is a trademark of Intel Corporation. Throughout this manual the name is used as a synonym for the IEEE 796 Microcomputer System Bus Standard, which is derived from the Multibus.

The convention used here corresponds to the Multibus convention as follows:

CT Convention	Multibus Convention	IEEE 796 Convention
RD-	RD/	RD*
RD+	RD	RD

In all other respects, our convention is the same as the Multibus convention.

REFERENCES

There is a reference section at the end of most chapters in this manual. These sections contain a variety of lists summarizing hardware-related functions. The appendices at the end of the manual contain additional reference material.

Since the system contains several programmable devices whose hardware functions and software interfaces are only briefly summarized in this manual, readers are likely to want occassional reference to the following manufacturer's literature:

Intel 8086 Family User's Manual
Intel Component Data Catalog
Zilog Z80A-SIO Technical Manual

Several new terms are introduced in the course of this manual. Generally, they are explained when first used but the Glossary at the end of the manual gives explanations of these terms.

SCHEMATICS

Schematic diagrams are included in each major section. Also, updated schematics as of January 1983 are included in Appendix G.

For use with CPU boards 60-00002-00 and 60-00036-00:

Total System Capacity	16K I/O Memory Board	64K I/O Memory Board	RAM Expansion Board
128K	128K		0
160K	128K		32K
192K	128K		64K
224K	128K		96K
256K	128K		128K
384K	128K		256K (64K chips)
512K	128K		384K (" ")
640K	128K		512K (" ")

For use with CPU board 60-00110-00:

Total System Capacity	16K I/O Memory Board	64K I/O Memory Board	RAM Expansion Board
384K*	128K		256K
384K		384K	
512K		384K	128K
512K		512K	
640K		384K	256K
768K		512K	256K
768K		384K	384K
1 Mb†		512K	512K

*This configuration can also be implemented using CPU boards 60-00002-00 and 60-00036-00.

†32 kilobytes of the address space must be reserved for permanent ROM space. Also, 160 kilobytes of the address space must be reserved for ROM space if the optional ROM Expansion board is used.

Note: For CPU board switch settings, see Appendix C.

Figure 2-9. RAM Configurations (kilobytes).

Typically, the operating system will write the entire contents of memory to disk upon parity-error detection and bootstrap a new version of the operating system.

The bottom 32 kilobytes of RAM, where the operating system typically resides, can be write-protected by setting a bit in the I/O Control Register (IOCR). If a write is attempted into this area, it is prevented and a non-maskable interrupt to the CPU is generated.

Multibus/Local-Bus Memory Mapping

The processor board contains a set of switches which define memory-space windows for local and Multibus masters. The windows determine whether memory resources on the Multibus or on the local bus will be addressed when an address is generated by a master. These windows are illustrated in Figure 1-4 of the prior chapter. Three choices of windows are available for local-bus masters, and four choices are available for Multibus masters.

This scheme of windowing is intended to facilitate communication across the Multibus interface with either 8-bit or 16-bit microprocessor boards on the Multibus. It also tends to minimize the amount of physical memory chips needed for high-address communication. A small and large window are available in both directions.

The small window is generally intended for inter-processor communication. On the Multibus side, this window falls within the 64-kilobyte address space of 8-bit boards without interfering with the board's ability to access its own low-end or high-end operating memory. On the local-bus side, there will always be some RAM at the low end of the memory space where communication message buffers are located and Multibus masters will be able to access these locations.

The large window is generally intended for buffering of large I/O devices, such as tape drives. The method used for shifting the window across the Multibus interface simply involves forcing the high-order address bits one way or another.

Pin	Signal
67	IOB1+
68	IOB0+
69	
70	IOCS-
71	NMI+
72	PICCS-
73	MEMCLK+
74	TEST
75	
76	IOW-
77	EOP-
78	VIDACK-
79	PERINT+
80	MWINH-
81	TO+
82	MBIO-
83	RESET-
84	PAREN+
85	
86	ADRF-
87	ADRE-
88	ADRD-
89	ADRC-
90	ADRB-
91	ADRA-
92	ADR9-
93	ADR8-
94	ADR7-
95	
96	ADR6-
97	ADR5-
98	ADR4-
99	ADR3-
100	ADR2-
101	ADR1-
102	ADR0-
103	DATF-
104	DATE-
105	
106	DATD-
107	DATC-
108	DATB-
109	DATA-
110	DAT9-
111	DAT8-
112	DAT7-
113	DAT6-
114	DAT5-
115	
116	DAT4-
117	DAT3-
118	DAT2-
119	DAT1-
120	DAT0-

Jumpers

Name	Function
A-C	Asynchronous READY
B-C	Synchronous READY

Switches

Switch	Bit	Function
1	1	Close for 4 Megahertz DMA.
1	2	Open for slow memory access (for debugging only).
1	4	Open for synchronous CPU and memory (for debugging only).
2	1	Close for Multibus slave region at greater than 512K.
2	4	Open for 32K to 48K multibus slave region.
3	1	Close for 512K multibus master boundary.
3	2	Close for 768K multibus master boundary.
3	3	Close if mainframe generates Multibus CCLK.
3	4	Close if mainframe generates Multibus BCLK.
4	1	Close if multibus master boundary is 768K.
4	2-4	Memory configuration. (See Figure 2-9.)
5	1	Close for 2364 and 2764 ROM types.
5	2	Close for 2316 and 2716 ROM types.
6	1	Close for no ROM expansion.
6	2	Open for no ROM expansion.
6	3	Close for no Multibus master memory access.
6	4	Close to always assert Multibus CBRQ.

The Memory Addressing Decode PROM

*

The CPU board has a 256 x 4 PROM on it that determines what rows of RAMs to enable when, and that tells the memory controller how much memory there is. The PROM determines this information based on the setting of switches at S4 on the CPU board. One of two memory addressing decode PROMS is used, depending upon whether a 16 kilobit or a 64 kilobit RAM is used. The part numbers for CPU boards used with the 16K I/O Memory board are 60-00002-00 and 60-00036-00. The part number for

the CPU board used with the 64K I/O Memory board is 60-00110-00. *

LED Indicators

LED	Meaning
CR1	Bus inactive
CR2	DMA active
CR3	Multibus active
CR5	Non-maskable interrupt
CR6	Interrupt

Test Points

Point	Meaning
TP 1	High during bus timeouts.
TP 2	Low when a DMA cycle is in progress.
TP 3	High a refresh is in progress. Normally oscillates at 12.8 khz.
TP 4	Ground to prevent refresh.
TP 5	High when a non-refresh memory cycle is in progress.

I/O-Port Address vs. Functions

address	logic	write reg.	read reg.
0	DMA	reserved	reserved
2	DMA	reserved	reserved
4	DMA	Comm. address	Comm. address
6	DMA	Comm. count	Comm. count
8	DMA	Disk address (low 16 bits)	Disk address
A	DMA	Disk count	Disk count
C	DMA	Video address	Video address
E	DMA	Video count	Video count
10	DMA	Command	Status
12	DMA	Request	-
14	DMA	Set/Reset Mask	-
16	DMA	Mode	-
18	DMA	Clear flip-flop	-
1A	DMA	Clear	-
1C	DMA	Mask	-
20	8259A	ICW1, OCW2, OCW3	IRR, ISR, INT Level
22	8259A	OCW1, ICW2, ICW3 ICW4	Mask

Device Pin Functions

The following several pages describe the pin functions of the complex ICs on the processor board.

Device Pin Functions: 8086 **HMOS MICROPROCESSOR**

The Intel 8086 is a new generation, high performance microprocessor implemented in N-channel depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. 8086 features include the following:

- o Direct addressing capability to 1 MByte of memory
- o Assembly language compatible with 8080/8085
- o 14 word, by 16 bit register set with symmetrical operations
- o 24 operand addressing modes
- o Bit, byte, word, and block operations
- o 8- and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
- o 5 MHz clock rate (8 MHz for 8086-2 (4MHz for 8086-4)
- o Multibus system compatibility

Pin functions tabulated below assume that the 8086 has been configured in its MAXIMUM mode, that is, the MN pin has been strapped to ground.

5. I/O-MEMORY BOARD

OVERVIEW

The I/O-Memory board is one of two mandatory boards which plug into the mainframe motherboard to implement the minimum-configuration mainframe. It contains main RAM plus control circuitry for all the I/O facilities except for the video logic and the mass storage subsystem.

OPERATION BY LOGIC BLOCK

Figure 5-1, shows how the major logic blocks relate to each other and how they participate in the flow of data on this board. The primary references, however, are the two schematics at the end of this chapter. The first schematic shows the 16K I/O Memory board; the second shows the 64K I/O Memory board. As in the previous chapter, frequent references are made to schematic page and zone numbers.

The RAM Array

The 7 address lines of the RAM ICs are multiplexed, so that 14 address bits can be represented with 7 pins. The chip is organized as a square matrix of 128 rows x 128 columns. Each row/column combination gives the address of 1 bit, or cell of memory.

The RAS- (row address strobe) signal has two functions: it latches the row address on the 7 address pins and it accesses the specified row of 128 cells. The CAS- (column address strobe) signal also has two functions: it latches the column address, and it performs the data operation, read or write, on the one cell specified by the column address of the 128 cells already accessed by RAS-. A write cycle is caused if the WE- pin is asserted at the leading edge of CAS-. The write data at the data input pin of the chip is latched by the leading edge of CAS-. A read cycle is caused if the WE- pin is inactive at the leading edge of CAS-. The read cycle causes the data from the selected cell to be driven on the chip's output pin.

The memory chips used are dynamic RAMs. Data is stored in parasitic capacitance that must be re-charged every 2 milliseconds to prevent leakage from destroying the contents of the memory.

Each time RAS- is asserted the entire 128-cell row corresponding to the state of the address pins is accessed. Whenever the cell is accessed it is re-charged.

In order to insure that all cells of the chip are refreshed (re-charged) every 2 milliseconds there is special refresh circuitry on the processor and I/O Memory boards. This circuitry works by issuing a RAS- every 12.8 microseconds and causing a counter to generate each different row address. CAS- is not issued during refresh, so no data is transferred.

64K RAMs work similarly to the 16K RAMs, except that there are sixteen address bits (one of the power supply pins of the 16K RAM being used as the extra address pin required for the 64K part) and the array is 256 rows of 256 columns.

The RAM array (p1) on the I/O Memory board is organized as 4 banks of 18 chips each. Each bank

of 18 chips corresponds to a word. Because the memory can be accessed a byte at a time, each byte has its own parity bit. So one word is represented as two 9-bit "bytes".

All 72 chips in the array have the same RAS- signal. Bank selection is done by asserting only one of the CAS- signals (CAS0-, CAS1-, CAS2-, CAS3-,). The data-in and data-out pins of each chip are tied together, making a bidirectional data bus (RAD0+ - RADF+). Each data bus bit is connected to 4 chips, consisting of the corresponding bit of each word in all 4 banks. The parity bits HIP+ (high-byte parity) and LOP+ (low-byte parity) are connected in the same fashion. The seven address pins (MAD1+ - MAD7+ are connected in parallel to all 72 chips. On the 16K I/O Memory board, the signal MAD8+ is connected to +5 at jumper E-F (p2zB6). On the 64K I/O Memory board, MAD8+ is used as an address bit. There are two write enable signals, RAHIWE- (high or odd byte write enable) and RALOWE- (low or even byte enable) which cause writing in either the low byte, the high byte, or both. Again, for writing, CAS- selects the particular bank written. Each write enable signal goes to 36 RAM chips.

The RAS- and CAS- signals for read, write and refresh are generated in the memory control of the processor board. When they come on to the I/O Memory board they are called RARAS- (RAM array row address strobe) (p2zD8) and CAS0- to CAS3- (p1zC8), corresponding to banks 0 through 3. On the 16K I/O Memory board, RARAS- is gated at 15H-11 (p2zB5) so that only refreshes and accesses to the I/O Memory board (as opposed to the RAM Expansion board) generate the signal BD1RAS-. BD1RAS- connects to the RAS- pins of the RAM IC's. On the 64K I/O Memory board, RARAS- is gated to the RAMs RAS- inputs at buffer 25C (p2zD7) by BDIEN-. BDIEN- is the ORed result of BDIRAM- or RFGO- at 13H-11 (p1zC5). RARAS- is also inverted at 14E-11 and used to clock two D-flip-flops at 15E (p1zA7). RFGO- indicates that a refresh is in progress and BD1RAM- (from the processor board) indicates the I/O Memory board RAM is being addressed.

There are three sources for the address driven on the RAM chip address pins, the row address (15G (p2zA7)), the column address (14G (p2zB7)), and the refresh row (15F (p2zC7)). On the 16K I/O

Memory board, the selection of which address driver is enabled is made by the high speed decoder consisting of 14E-6, 8, 11, 13H-11 and 14H-4 and 13 (p2zA7). The RFGO- signal, when active, enables 15F and disables 14G and 15G. The COLMPX- (column multiplex) signal causes the row driver (15G) to disable and the column driver (14G) to enable. On the 64K I/O Memory board, COLMPX- is sent directly to the pin 1 selector inputs of 14G and 15G. RFGO- is buffered at 9E-12 and inverted at 14H-4 to enable 14G and 15G. COLMPX- and RFGO- come from the RAM controller on the processor board. RFDONE- from the processor board indicates that a refresh cycle has completed and causes the refresh address counters 13F and 14F (p2zC7) to increment.

On the 16K I/O Memory board, data to and from the RAM array is buffered from the MEM bus (MEMO+ - MEMF+) by the transceivers at 10E (p2zD4) and 11E (p2zC4). The direction of the transceivers is established by the signal READ- which is a buffered MR- (memory read) signal. The enable for the high (odd) byte driver is HIEN- and for the low (even) byte is LOEN-. HIEN- is asserted when the I/O Memory board RAM is addressed (BD1RAM- asserted at 13E-3 (p1zA6)) and either a read is in progress (MR- active) or the high-order byte write enable is active (RAHIWE-). LOEN- is asserted when the I/O Memory board RAM is addressed and either a read is in progress or the low-order byte write enable is active (RALOWE-).

On the 64K I/O Memory board, two pairs of buffers transfer data to and from the RAM array. Buffers 10.5E (p2zD4) and 13E buffer data from the RAM array and are enabled by READ- from page 1 of the schematic. Buffers 10E and 11E are enabled by RDEN-, also from page 1 of the schematic.

Disk Control Interface (DCI)

The disk control interface drives and receives the signals that interface the mainframe to the mass storage subsystem.

During I/O write (IOW-) the latching drivers at 9F and 9H (p3zB4) latch output data. This is done by the BIOW- (buffered IOW-) signal from 6H-3, inverted at 5F-12 (p3zC4). After a delay by R11, C6, and 5F-8, the buffer 6H-16 (p3zB4) makes WRSTB- (write strobe) which goes to the disk

controls located in the mass storage subsystem. After another delay by R10, R32, C5, and 5F-6 (p3zC6), the data is driven to the disk controls by 9F and 9H (p3zB4) (BUSO+ - BUSF+). The delays ensure enough data hold and setup time on BUSO+ - BUSF+ for the MOS floppy disk controller.

IOR- is buffered at 6H-12 (p3zB4) to make BIOR- (buffered I/O read). The gate at 10G-6d (p3zB5) enables the BUS to MEM drivers (8F and 8H (p3zC4)) and sends a RDSTB- (read strobe) to the disk controls. 10G-6 is asserted when BIOR- is present and one of the disk controls is addressed (DCI1- or DCI2- active) or disk DMA is active (DISKACK- active). The address decodes, DCI1- and DCI2-, are ORed at 5H-11 (p3zA7) and then they are ORed with DISKACK+ at 4E-13. DISKACK- comes from the DMA logic on the processor board.

The BMR- (buffered memory read) signal at 13H-3 (p3zA3) goes to the disk controls to synchronize their DMA requests. It is a buffered copy of MR-.

The CNTRL- signal to the disk controls is used to address the control and status registers of the disk controls, rather than the data registers. It is asserted by gate 5H-8 (p3zA6) when DMA is not in progress (DISKACK- inactive) and local address bit LA1+ is high.

The DREQ- (DMA request) signal from the disk controls is buffered at 5F-10 (p3zB5) to make DISKRQ+ which goes to the DMA logic of the CPU board.

The INRQ- (interrupt request) signal from the disk controls causes a level-7 interrupt (INT7-) when gate 3C-4 (p3zB6) is asserted.

The signal ACK- is a bidirectional acknowledge signal between the DCI and the disk controls. During DMA cycles, DISKACK- from the processor board causes gate 5H-3 (p3zA6) to assert ACK-. The disk controls use this as their DMA acknowledge. During non-DMA activity, the disk controls assert ACK- whenever they are addressed (DCI1- or DCI2- active). If a disk control does not assert ACK- when addressed, gate 5H-6 (p3zA6) will cause DCIRDY+ to go false. This causes a bus timeout in the ready logic of the processor board.

The signal EOP- (end of process) from the DMA logic of the processor board indicates that a DMA block is complete. This is buffered at 6H-18 (p3zB4) to generate BEOF- which goes to the disk controls.

The two disk control I/O address decodes, DCI1- and DCI2- are buffered at 6H-5, -7 (p3zB4) to generate SELW- (select winchester) and SELF- (select floppy) for the disk controls.

Inputting from port 74, used for diagnostics, causes the most recent 16 bits of information outputted (IOW- active) to be echoed. This is used to check the BU80+ - BUSF+ drivers and receivers. WRAPDCI+ is asserted at 13H-8 (p4zC3) when port 74 is read (IOR- active, DC12- active, LA2+ active). At 6H-19 (p3zB4), WRAPDC1+ causes the SELF- signal to be disabled to prevent the floppy control from driving BUS0+ - BUSF+ during the input from 74. In addition, 6H-19 causes 6H-9 to be disabled, which in turn causes the DCI drivers 9F and 9H (p3zB4) to be enabled, driving BUS0+ - BUSF+. Through the normal mechanism of reading the disk control ports, gate 10G-6 (p3zB5) causes the data on BUS0+ - BUSF+ to be driven onto MEM0+ - MEMF+.

When the power fail detect circuit has detected an error, the POWEROK- signal will go inactive. This causes driver IC-9 (p3zC2) to make the ENBL- signal to the disk controls inactive, disabling the disk controls.

I/O Address Decode

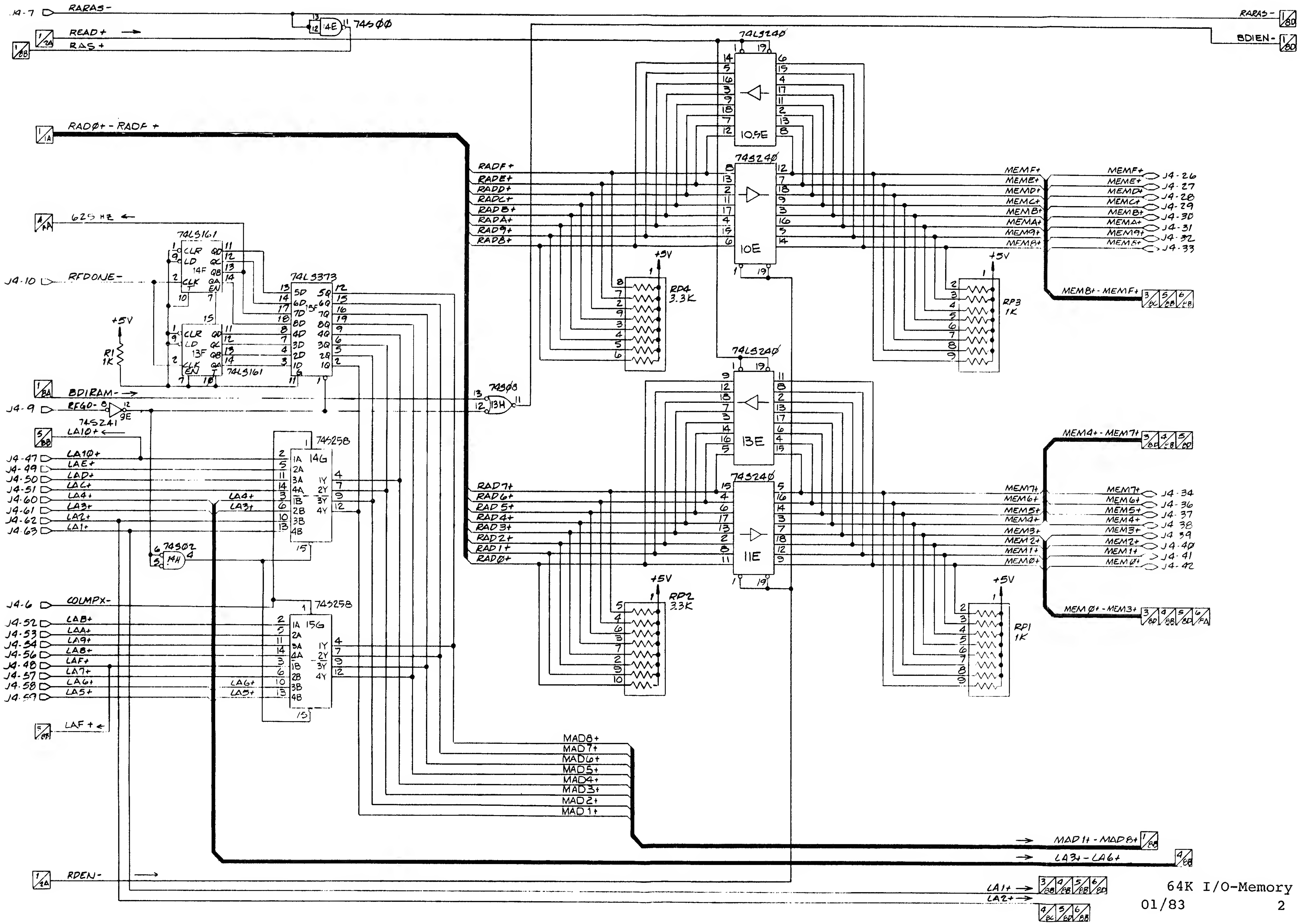
The I/O address decode logic generates the signals shown in Figure 5-2. 12E-8 (p4zB4) ORs several of the decodes to generate FASTIO+. FASTIO+ is used on the processor board to indicate that the addressed I/O device does not require wait states. For all other I/O device addresses, IOBCS+ goes active at 13G-6 (p4zB3). This does two things on the processor board. It causes wait states for the I/O instructions that refer to those devices, and for input instructions it causes the data to come from the I/O bus (IOB0+ - IOB7+) instead of directly from the MEM bus.

The I/O Control Register (IOCR)

The IOCR and its associated logic control the several reasons for generating level-4 interrupts and non-maskable interrupts. The IOCR is also used to control parity, memory write protect, and Multibus I/O addressing. The IOCR consists of drivers 11F and 11H, latch 10H, and flip-flops 9G-9, 9G-5, 8G-9, 7G-9 and 6F-9 (p5). The high-order 8 bits of IOCR, corresponding to MEM8+ - MEMF+ are control bits, and the low-order 8 bits corresponding to MEM0+ - MEM7+ are status bits. The control bits are loaded into register 10H from MEM8+ - MEMF+ when there is an output (IOW-) to the IOCR I/O address as described in the I/O address decode section. The register can be read back when ICTLRDC- goes active (IOR- and IOCR address) causing the driver at 11H to drive the IOCR contents onto MEM8+ - MEMF+. Simultaneously ICTLRDC- causes the IOCR status bits to be driven onto MEM0+ - MEM7+ through 11F.

Signal name	Address	Strobe	Source	Device Addressed
PCICS	38-3F	none	12G-7 (p4zB5)	8251A USART
COMMIA-	30-37	none	12G-9 (p4zB5)	SIO Interrupt Acknowledge
TIMERCS-	28-2F	none	12G-10 (p4zB5)	8253 Programmable Timer
PICCS-	20-27	none	12G-11 (p4zB5)	8259A Interrupt Controller
DCI1	78-7F	none	12F-7 (p4zA5)	Hard disk control
DCI2-	70-77	none	12F-9 (p4zA5)	Floppy disk control
DMACTCS-	68-6F	none	12F-10 (p4zA5)	DMA Extended Address Register
COMMF-	60-67	none	12F-11 (p4zA5)	Comm Extended Control Register
GACCS-	58-5F	none	12F-12 (p4zA5)	Video Global Attribute Register
COMMS-	48-4F	none	12F-14 (p4zA5)	SIO communication chip
PPICS-	40-47	none	12F-15 (p4zA5)	The LEDs/Speaker/and switches
LPTRDC	50-51	IOR-	11G-4 (p4zB3)	Line printer status
RDLOPEA-	52-53	IOR-	11G-5 (p4zB3)	Low order parity error address
RDHIPEA-	54-55	IOR-	11G-6 (p4zB3)	High order parity error address
ICTLRDC-	56-57	IOR-	11G-7 (p4zB3)	IOCR reading
DMACS-	00-1F	none	6E-8 (p4zB3)	8237 DMA controller
LPTWDC-	50-51	IOW-	11G-12 (p5zB7)	Line printer output
ICTLWDC-	56-57	IOW-	11G-9 (p5zB7)	IOCR writing
WRAPDCI+	74-77	IOR-	13H-8 (p4zC3)	DCI wraparound (diagnostics)

Figure 5-2. I/O Address Decode Signals



64K I/O-Memory board

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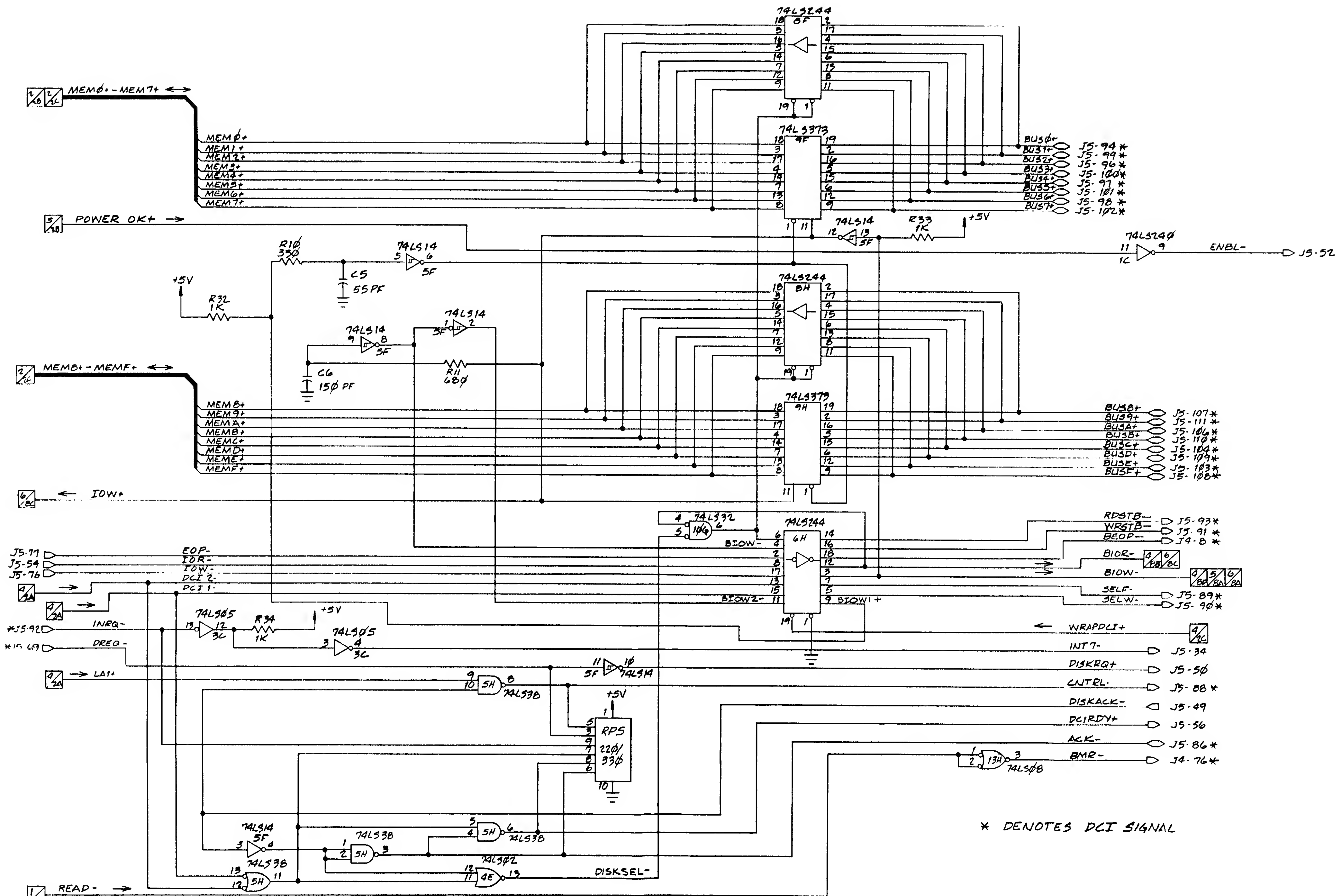
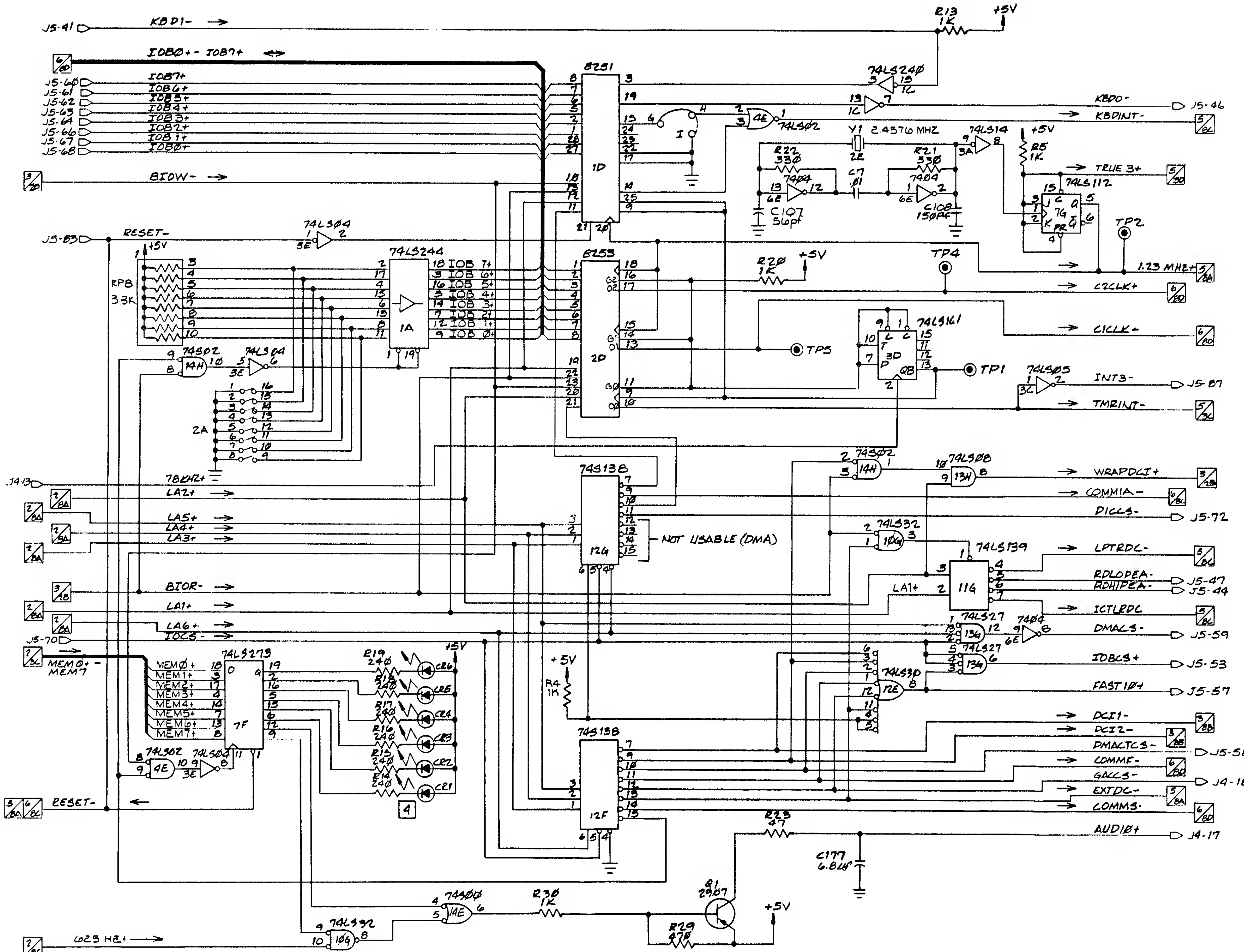
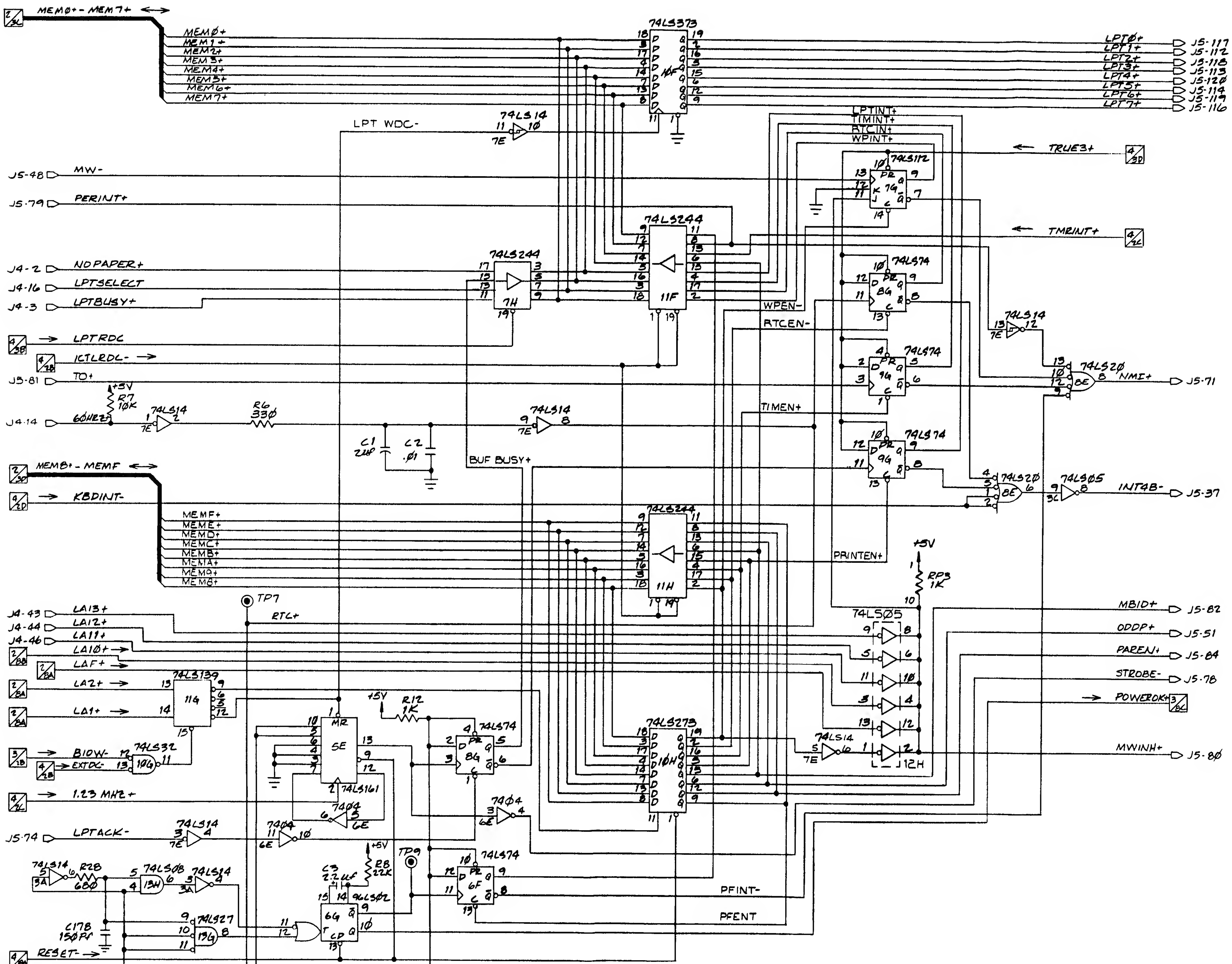
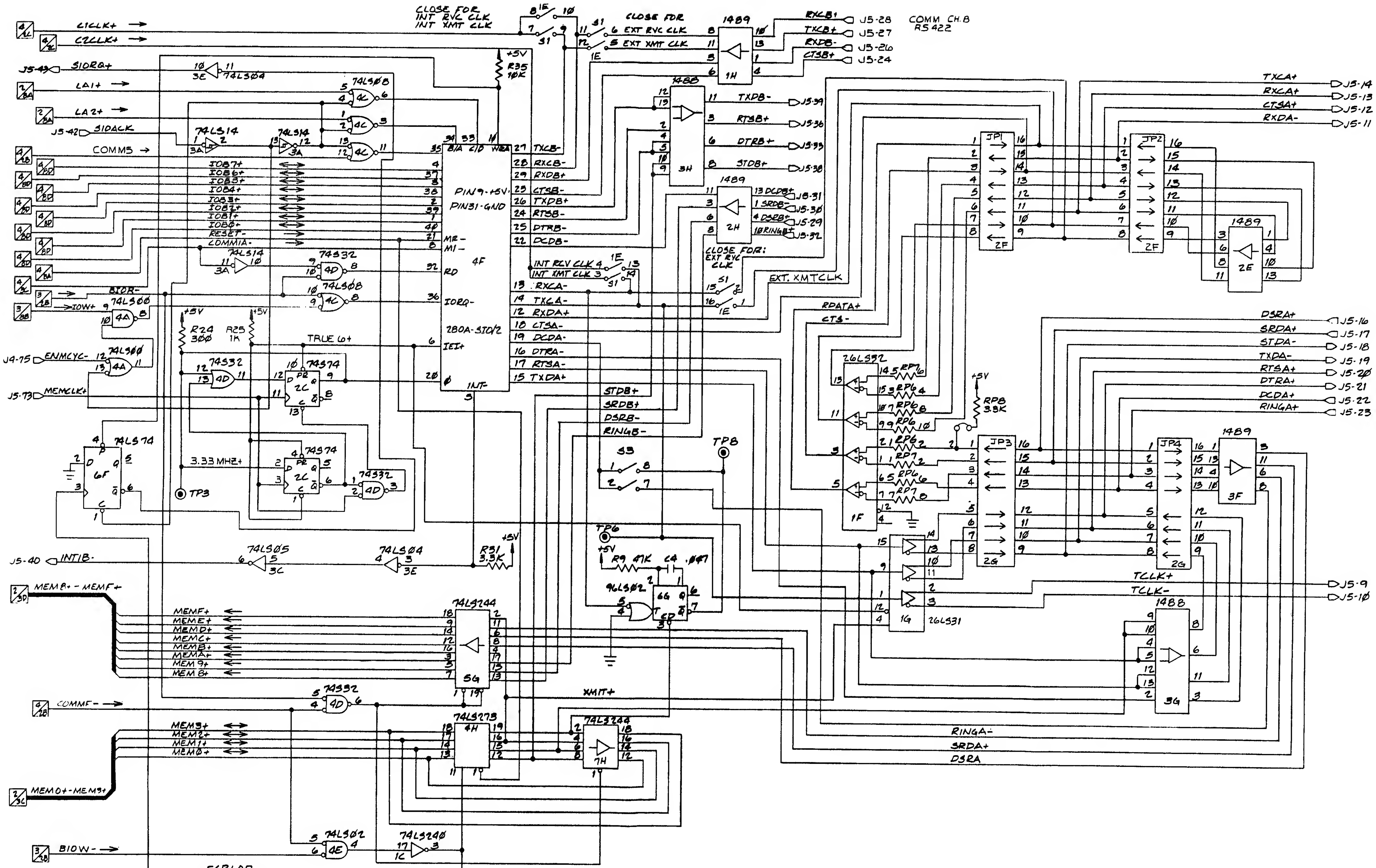

MEMØ+ - MEM7+
POWER OK+
MEM8+ - MEMF+
IOW+
74LS244
74LS373
74LS14
74LS240
ENBL-
74LS32
BIOW-
BIOW2-
BIOW1+
RDSTB-
WRSTB-
BEOP-
BIOR-
BIOW-
SELF-
SELW-
EOP-
IOR-
IOW-
DCI 2-
DCI 1-
INRQ-
DREQ-
LA1+
74LS05
WRAPDCI+
INT7-
DISKRQ+
CNTRL-
DISKACK-
DCIRDY+
ACK-
BMR-
74LS38
74LS02
74LS08
RP5
220/330
DISKSEL-
READ-
* DENOTES DCI SIGNAL


KBDI-
IOBØ+ - IOB7+
IOB7+
IOB6+
IOB5+
IOB4+
IOB3+
IOB2+
IOB1+
IOBØ+
BIOW-
RESET-
8251
8253
74LS244
74LS240
74LS02
74LS14
74LS112
74LS161
74LS05
74LS04
74S02
74S138
74LS08
74LS32
74LS139
74LS27
74LS30
74LS273
74S00
74LS32
Y1 2.4576 MHZ
R13 1K
R5 1K
R22 33Ø
R21 33Ø
C107 56pf
C108 15ØPF
R2Ø 1K
RP8 3.3K
TRUE 3+
1.23 MHZ+
C2CLK+
C1CLK+
TP1
TP2
TP4
TP5
INT3-
TMRINT-
KBDO-
KBDINT-
78KHZ+
LA2+
LA5+
LA4+
LA3+
LA1+
LA6+
BIOR-
IOCS-
NOT USABLE (DMA)
WRAPDCI+
COMMIA-
DICCS-
LPTRDC-
RDLOPEA-
RDHIPEA-
ICTLRDC
DMACS-
IOBCS+
FAST IØ+
DCI1-
DCI2-
DMACTCS-
COMME-
GACCS-
EXTDC-
COMMS-
AUDIØ+
C177 6.8μF
R23 47
Q1 2907
R3Ø 1K
R29 47Ø
R4 1K
MEMØ+ - MEM7
MEMØ+
MEM1+
MEM2+
MEM3+
MEM4+
MEM5+
MEM6+
MEM7+
R19 24Ø
R18 24Ø
R17 24Ø
R16 24Ø
R15 24Ø
R14 24Ø
CR1
CR2
CR3
CR4
CR5
CR6
625 HZ+
+5V
J5-41
J5-46
J5-83
J5-87
J5-72
J5-47
J5-44
J5-59
J5-53
J5-57
J5-58
J5-70
J4-13
J4-18
J4-17

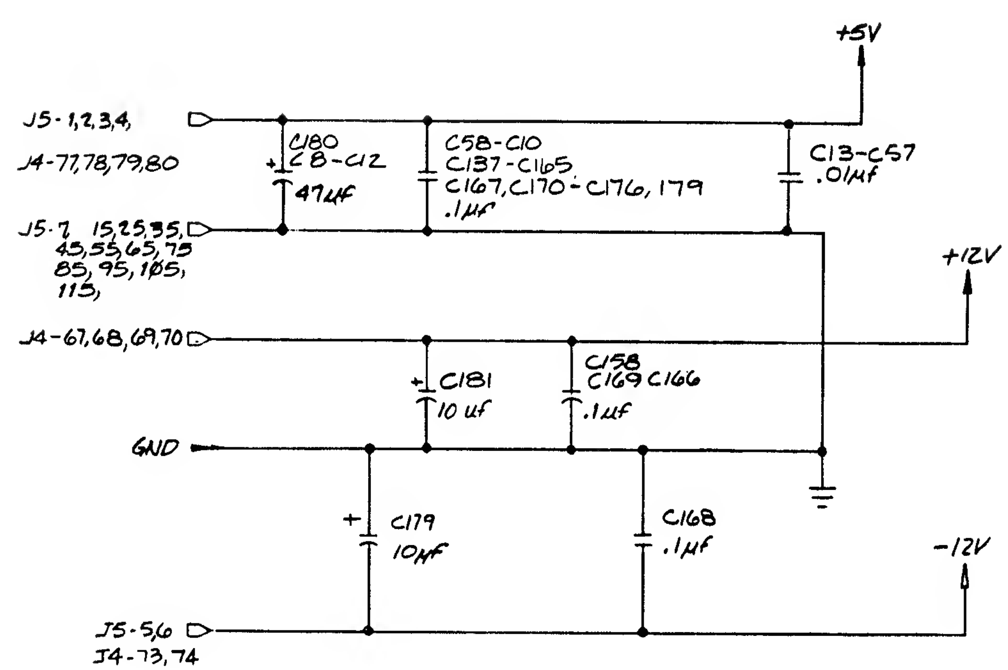

MEM0+ - MEM7+
74LS373
LPT WDC-
74LS14
MW-
PERINT+
NOPAPER+
LPTSELECT
LPTBUSY+
LPTRDC
ICTLRDC-
TO+
60HZ
74LS244
74LS112
74LS74
74LS20
74LS05
74LS139
74LS32
74LS161
74LS04
74LS08
74LS27
74LS273
96LS02
LPTINT+
TIMINT+
RTCINT+
WPINT+
TRUE3+
TMRINT+
WPEN-
RTCEN-
TIMEN+
BUF BUSY+
PRINTEN+
NMI+
INT4B-
MEMB+ - MEMF
KBDINT-
LA13+
LA12+
LA11+
LA10+
LAF+
LA2+
LA1+
BIOW-
EXTDC-
1.23 MHZ+
LPTACK-
RESET-
RTC+
TP7
TP9
PFINT-
PFENT
MBID+
ODDP+
PAREN+
STROBE-
POWEROK+
MWINH+
LPT0+
LPT1+
LPT2+
LPT3+
LPT4+
LPT5+
LPT6+
LPT7+


CLOSE FOR INT RVC CLK INT XMT CLK
CLOSE FOR EXT RVC CLK EXT XMT CLK
COMM CH.B RS422
C1CLK+
C2CLK+
SIORQ+
LA1+
LA2+
SIDACK
COMMS
IOB7+ IOB6+ IOB5+ IOB4+ IOB3+ IOB2+ IOB1+ IOB0+ RESET- COMMIA-
BIOR-
IOW+
ENMCYC-
MEMCLK+
PIN 9 - +5V PIN 31 - GND
Z80A-SIO/2
TRUE LO+
3.33 MHZ+
TP3
INTIB-
MEMB+ - MEMF+
MEMF+ MEME+ MEMD+ MEMC+ MEMB+ MEMA+ MEM9+ MEM8+
COMMF-
MEM3+ MEM2+ MEM1+ MEM0+
MEM0+-MEM3+
BIOW-
ECRLOD-
XMIT+
TXDB- RTSB+ DTRB+ STDB+
RXCB+ TXCB+ RXDB- CTSB+
DCDB+ SRDB- DSRB+ RINGB+
CLOSE FOR: EXT RVC CLK
EXT. XMTCLK
RDATA+ CTS-
TXCA+ RXCA+ CTSA+ RXDA-
DSRA+ SRDA+ STDA- TXDA- RTSA+ DTRA+ DCDA+ RINGA+
TCLK+ TCLK-
RINGA- SRDA+ DSRA
TP6 TP8
74LS04 74LS08 74LS14 74S32 74LS00 74S74 74LS74 74LS05 74LS244 74LS273 74LS02 74LS240 96LS02 26LS32 26LS31 1488 1489

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS, 1/4W 5 %
2. COMPACITANCE VALUES ARE IN PICOFARADS.
3. ALL DEVICES ARE STANDARD 7 & 14, 8 & 16 AND 10 & 20 GROUND & POWER CONNECTIONS.
4. ALL DIODES ARE TYPE FLV560.

POWER AND GROUND LOCATOR CHART					
REF. DES.	DEVICE TYPE	+5V	GND	+12	−12
5A-22A 5B-22B 5C-22C 5D-22D	416D-4	8	16		
4F	Z80A-SIO/2	9	31		
1D	8251	26	4		
3H, 3G	1488		7	14	1



SPARE GATES		
REF DESIG.	DEVICE TYPE	NO. OF GATES

REFERENCE DESIGNATION	
LAST USED	NOT USED
RP7	
R34	
C181	C109-C136
JP4	
CR6	
Y1	
J5	J1-J3

WORKSTATION HARDWARE MANUAL

Volume 2

Specifications Subject to Change.

First Edition Revised (April 1981) A-09-00016-01-B

CONTENTS: Volume 2

10. Video Monitor (CRT)

11. Console Switches

12. Power Supply

13. Communications I/O Processor Board

LIST OF FIGURES

14. Multiline Communications Processor Board

To be supplied.

APPENDIX C

WORKSTATION SWITCH AND JUMPER SETTINGS

CPU BOARD SWITCHES

The functions of each of the switches on the CPU board are listed below.

S1

Bit	On	Off
1	4 MHz DMA	5 MHz DMA
2	no wait states	one wait state
3	not used	not used
4	5 MHz 8086	3.3 MHz 8086

S2

Bit	On	Off
1	Multibus-to-CT window at 512K	no Multibus-to-CT window at 512K
2	not used	not used
3	not used	not used
4	no Multibus-to-CT window at 32K	Multibus-to-CT window at 32K

S3

Bit	On	Off
1	CT-to-Multibus window at 512K	CT-to-Multibus window at 768K
2	CT-to-Multibus window at 768K	CT-to-Multibus window at 512K
3	CT generates CCLK-	external CCLK- generation
4	CT generates BCLK-	external BCLK- generation

S4 (for use with 16K I/O Memory board and CPU board numbers 60-00002-00 or 60-00036-00) *

Bit	On	Off
1	640K RAM total	256K RAM total 384K RAM total 512K RAM total
2	640K RAM total	256K RAM total 384K RAM total 512K RAM total
3	256K RAM total 512K RAM total 640K RAM total	384K RAM total

Bit	On	Off
4	256K RAM total 384K RAM total	512K RAM total 640K RAM total

S4 (for use with 64K I/O Memory board and CPU board number 60-00110-00)

1	640K RAM total 768K RAM total 1 Mb RAM total	384K RAM total 512K RAM total
2	384K RAM total 512K RAM total 640K RAM total	384K RAM total 768K RAM total 1 Mb RAM total
3	384K RAM total 768K RAM total	384K RAM total 512K RAM total 640K RAM total 1 Mb RAM total
4	384K RAM total 384K RAM total 512K RAM total 768K RAM total	640K RAM total 1 Mb RAM total

S5

1	2732 PROMs	2716 PROMs
2	2716 PROMs	2732 PROMs
3	not used	not used
4	not used	not used

S6

1	no PROM board	PROM board
2	PROM board	no PROM board
3	no CT-to-Multibus access	CT-to-Multibus access enabled
4	CBRQ- always asserted	CBRQ- from Multibus master

CPU BOARD JUMPERS

For workstations without 8087 coprocessors, a jumper from TP6 to ground must be installed. If an 8087 is used, there must be no jumper installed.

I/O-MEMORY BOARD SWITCHES

The functions of each of the switches on the I/O-Memory board are listed below.

S1

Bit	On	Off
1	Channel A external transmit clock	Channel A internal transmit clock
2	Channel A external receive clock	Channel A internal receive clock
3	Channel A internal transmit clock	Channel A external transmit clock
4	Channel A internal receive clock	Channel A external receive clock
5	Channel B external transmit clock	Channel B internal transmit clock
6	Channel B external receive clock	Channel B internal receive clock
7	Channel B internal transmit clock	Channel B external transmit clock
8	Channel B internal receive clock	Channel B external receive clock

S2

ID switch: For workstations with serial number A-8131A-0400 or lower, see the "Bootstrap ROM" section in the second edition (A-09-00014-02-A) of the System Programmer's Guide. For workstations with serial number A-8131B-0400 or higher, see the Release Notice for Common Boot ROM Firmware (A-09-00065-01-A).

S3

Bit	On	Off
1	internal carrier detect	external carrier detect
2	external carrier detect	internal carrier detect
3	not used	not used
4	not used	not used

I/O-MEMORY BOARD JUMPERS

For Channel A RS-232 operation, jumper plugs must be installed in JP2 and JP4 and not in JP1 and JP3.

For Channel A RS-422 operation, jumper plugs must be installed in JP1 and JP3 and not in JP2 and JP4.

On the 16K I/O Memory board, jumper E-F must be installed for proper operation.

RAM EXPANSION BOARD JUMPERS

If a 128K RAM Expansion Board is included, jumper A-C must be installed for 16K RAM operation.

MOTHERBOARD JUMPERS

A jumper plug must be installed in motherboard location U3 for cluster communications operation. This connects the 9-pin cluster communications connectors and protection diodes to Channel A. For workstations with a switch in U3, all 8 bits must be on.

For noncluster Channel A use, there must be no jumper plug in location U3, or if there is a switch, all 8 bits must be off.

APPENDIX D: MONITOR FORM OF THE IWS WORKSTATION

To be supplied.

APPENDIX E: IWS BOOTSTRAP ROMS

To be supplied.

APPENDIX F: IWS GRAPHICS CONTROL BOARD

LIST OF FIGURES

LIST OF TABLES

APPENDIX F: IWS GRAPHICS CONTROL BOARD

OVERVIEW

This appendix is for the engineer who writes service manuals, tests the IWS Graphics Control Board electronics, or writes (or modifies) system software for use with the IWS workstation. This appendix does not provide documentation to support modification of the Graphics Control Board hardware.

The IWS Graphics Board enhances the IWS workstation or the monitor form of the IWS workstation by providing medium-resolution graphics capabilities. Twin graphic display planes are provided, each with viewports of 656 by 510 pixels. The assignment of each pixel on the video display is mapped from a linear memory array consisting of 16 64-kilobyte dynamic RAMs.

The Graphics Control Board plugs into one of the Multibus slots in an IWS and is controlled by a Intel 8086-2 microprocessor executing ROM-resident firmware from 8 kilobytes of EPROM. Eight kilobytes of static RAM are provided to store command and status information for the microprocessor.

The "Architecture" section of this appendix describes the use of the address space on the Graphics Control Board, switch selection, the single Control Register, and the display planes.

The "Theory of Operations" section describes, at a component level, the operations of the circuitry on the Graphics Control Board.

ARCHITECTURE

The following aspects of the IWS Graphics Control Board architecture are discussed:

- The IWS Graphics Control Board has 1 megabyte of local address space accessible by the IWS CPU through a 64-kilobyte window in the Multibus address space. An Extended Address Register is used to provide four high-order address bits for the Graphics Control Board addresses.

- The Control Register provides several bits of control over the graphics hardware.

- The Graphics Control Board contains a local Intel 8086-2 microprocessor operating at 8 MHz from a program stored in 8 kilobytes of EPROM. Additionally, 8 kilobytes of static RAM is provided for storage of commands and status information.

- The two independently addressable display planes resident in dynamic RAMs store the graphics image (or bit map) displayed on the IWS video display. Each display plane is 1024 bits horizontally by 512 bit vertically.

Graphics Control Board Mapping and Local Addressing

As described in the "System Architecture" section of the Workstation Hardware Manual, the IWS CT Bus and the Multibus each have 1 megabyte of address space. Since the IWS has a maximum address range of 1 megabyte, a common area (a window) of mutually addressable space must be created on the CT Bus to allow the Multibus to be addressed.

Multibus Window

Similarly, the 1-megabyte address space on the IWS Graphics Control Board must be addressed through a 64-kilobyte window set on the Multibus by the SW2 switches on the IWS Graphics Control Board. Figure 2-1 below shows the relationship between the address space of the CT Bus and those of the Multibus and the Graphics Control Board Local Bus. With Convergent's current standard software, the Multibus mapping on the CT Bus

begins at 768 kilobytes, or C000:0h, and extends to 991 kilobytes or F7FF:Fh. This maps into a 224-kilobyte address space on the Multibus beginning at 0000:0. The IWS Graphics Control Board uses 64 kilobytes in this address space as its interprocessor communications window. The four switches at SW2 select the 64-kilobyte block of addresses to which the Graphics Control Board will respond. Table 2-1 below lists the switch settings for SW2. Convergent standard software supports 64-kilobyte windows beginning at CT-Bus locations C000:0h, D000:0h, and E000:0h.

Table 2-1. Multibus Memory Address Switch Settings.

SW2 1	2	3	4	Memory Address (h)	
OFF	OFF	OFF	OFF	0000:0-0FFF:F	*
OFF	OFF	OFF	ON	1000:0-1FFF:F	*
OFF	OFF	ON	OFF	2000:0-2FFF:F	*
OFF	OFF	ON	ON	3000:0-3FFF:F	
OFF	ON	OFF	OFF	4000:0-4FFF:F	
OFF	ON	OFF	ON	5000:0-5FFF:F	
OFF	ON	ON	OFF	6000:0-6FFF:F	
OFF	ON	ON	ON	7000:0-7FFF:F	
ON	OFF	OFF	OFF	8000:0-8FFF:F	
ON	OFF	OFF	ON	9000:0-9FFF:F	
ON	OFF	ON	OFF	A000:0-AFFF:F	
ON	OFF	ON	ON	B000:0-BFFF:F	
ON	ON	OFF	OFF	C000:0-CFFF:F	
ON	ON	OFF	ON	D000:0-DFFF:F	
ON	ON	ON	OFF	E000:0-EFFF:F	
ON	ON	ON	ON	F000:0-FFFF:F	

* indicates address range supported by Convergent standard software

Local Addresses

Figure 2-2 below shows the 1-megabyte address space for the Graphics Control Board. At the bottom, 8 kilobytes of the address space is the static RAM used by both the IWS CPU and the local CPU to pass command and status information. At address 4000:0h, 1 byte is allocated for the Control Register, which provides several hardware

control signals described below under "Control Register." Two display planes, each 64 kilobytes, reside at addresses 8000:0h and 9000:0h, respectively. The local 8086-2's 8-kilobyte program resides in EPROM, starting at address FE00:0h. All of the above local resources can be accessed by both the IWS and local CPU. Access by the IWS CPU is limited to word addressing and is slower than an access by the local CPU.

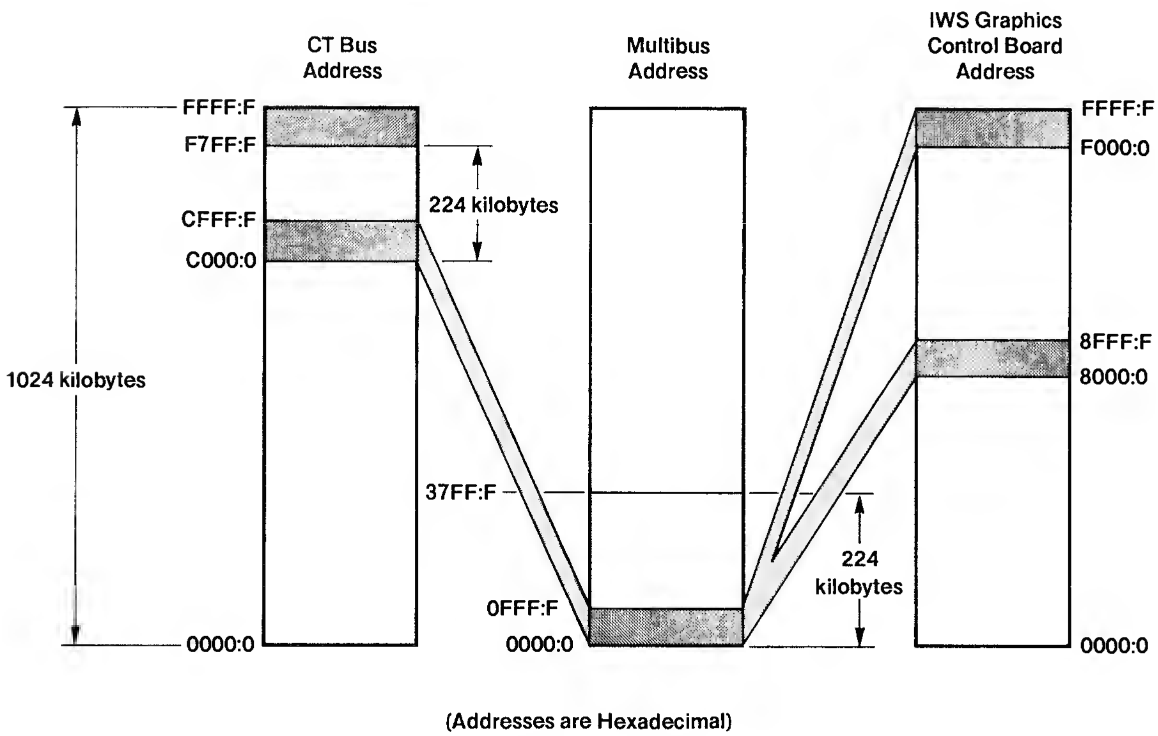


Figure 2-1. IWS Graphics Control Board Address Mapping.

Extended Address Register

Since the Multibus window to the Graphics Control Board is 64 kilobytes and the total address space on the Board is 1 megabyte, an Extended Address Register is used. As shown in Figure 2-3, the full 20-bit address consists of 16 least-significant bits from the Multibus and the four high-order bits from the complement of the Extended Address Register.

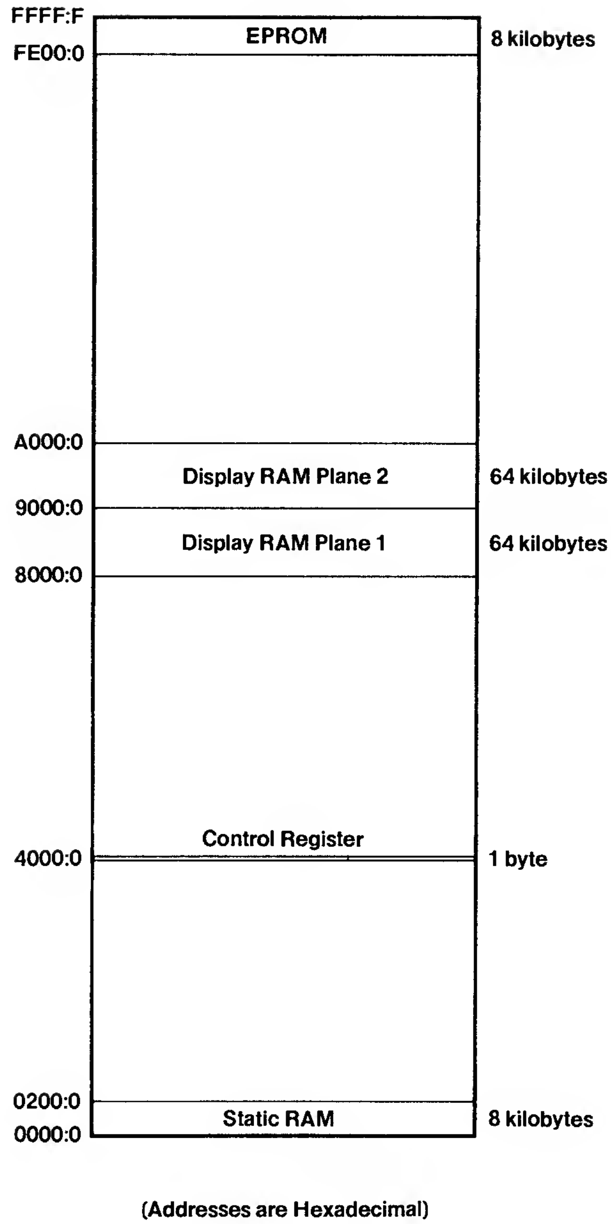


Figure 2-2. IWS Graphics Control Board Memory Address Space.

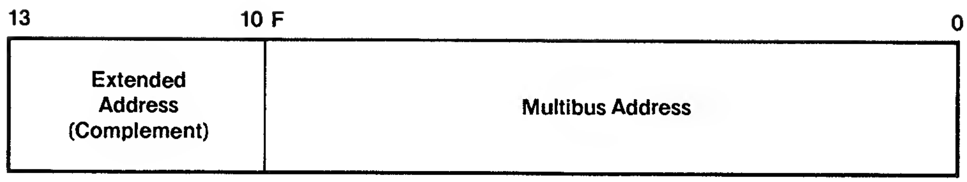


Figure 2-3. Multibus Addressing Scheme.

The Extended Address Register is a Multibus output port loaded by the IWS CPU. The contents of the register are loaded from the four least significant data bits. The Extended Address Register should only be written to and has an address that is selectable through switches at SW1. Current standard software accesses the Extended Address Register at port address 8030h. Table 2-2 below lists the address switch settings for SW1.

Table 2-2. Extended Address Register Port Switch Settings.

SW1 1	SW1 2	SW1 3	SW1 4	Register Address (h)	
OFF	OFF	OFF	OFF	XX00	
OFF	OFF	OFF	ON	XX10	
OFF	OFF	ON	OFF	XX20	
OFF	OFF	ON	ON	XX30	*
OFF	ON	OFF	OFF	XX40	
OFF	ON	OFF	ON	XX50	
OFF	ON	ON	OFF	XX60	
OFF	ON	ON	ON	XX70	
ON	OFF	OFF	OFF	XX01	
ON	OFF	OFF	ON	XX11	
ON	OFF	ON	OFF	XX21	
ON	OFF	ON	ON	XX31	
ON	ON	OFF	OFF	XX41	
ON	ON	OFF	ON	XX51	
ON	ON	ON	OFF	XX61	
ON	ON	ON	ON	XX71	

* indicates address supported by Convergent standard software

For an example of how the Extended Address Register is used, consider an IWS CPU read operation of the first address of the static RAM at address 0000:0. The IWS CPU must first address the Extended Address Register at port 8030h and then write the complement of the high-order address into it. Since the static RAM resides in the first 8 kilobytes of the Graphic Control Board's address space, the four high-order bits are all 0. Therefore, 0Fh is written into the Extended Address Register as the complement. To write to the Control Register at address 4000:0h on the Graphics Control Board, the complement of the address is 0FBh, where Bh is the contents of the Extended Address Register.

To summarize some common address complements for the Extended Address Register:

Table 2-3. Extended Address Register Complement Summary.

Byte Output (h)	Data Accessed
0FF	Static RAM
0FB	Control Register
0F7	Display Plane 1
0F6	Display Plane 2
0F0	EPROM

Control Register

The Control Register at address 4000:0h provides several control bits for the graphics hardware and can only be written to. Any attempt to read this register results in changing its contents to an indeterminant value. When the Graphics Control Board is reset, all of the bits in the Control Register are set to 0. The function of the bits in the Control Register are as follows:

Control Bit	Write Information
0	LOCBLANK- (Local Blank). When LOCBLANK- is 0, the graphics output is disabled. When 1, the video shift registers are enabled

Control Bit	Write Information
	and graphics information is sent to the Video Board.
1	80COL+ (80-Column Alphanumeric Mode). When 80COL+ is 0, the IWS is operating in the 132-column alphanumeric mode. When 1, the IWS is operating in the 80-column alphanumeric mode. This bit, set by software when the screen size is changed, determines the operation of the on-board phase-locked loop to provide a constant 26-MHz pixel clock to the Video Board.
2	Y9+ (Most Significant Display-Memory Address Bit). This bit is used to determine which of the two display planes is currently being displayed. When Y9 is 0, Display Plane 1 (address 8000:0h-8FFF:Fh) is being shown on the video display. When 1, Display Plane 2 (address 9000:0h-9FFF:Fh) is being shown on the video display.
3	MEMENB+ (Memory Enable). If MEMENB+ is 0, the display memory is disabled and cannot be accessed. If MEMENB+ is 1, the display memory can be accessed.
4	HBVIDEO+ (Half-Bright Video). This bit overrides the half bright video attributes from the Video Board. If HBVIDEO+ is 0, alphanumerics are being displayed on the video display and any half-bright video attributes are from the Video Board. When alphanumerics are disabled, HBVIDEO+ is set to 1 by the software to drive the display to all full-bright, overriding any half-bright attributes from the Video Board.
5-7	Unused.

Static RAM and EPROM

The 8 kilobytes of static RAM, starting at address 0000:0, is used for passing command and status information between the IWS CPU and the local CPU. The local CPU can address RAM at 8 MHz without incurring any wait states. RAM access by the IWS CPU depends on how long it takes the IWS CPU to acquire the Multibus. The RAM is only word-writable by the local CPU and word-addressable (writing and reading) from the Multibus.

The 8 kilobytes of EPROM starting at address FE00:0h contains the graphics firmware. The local CPU executes code out of EPROM at 8 MHz without incurring any wait states. The IWS CPU may read from EPROM but, as with static RAM, the access time depends on the Multibus acquisition time. The EPROM is byte-readable by the local CPU and word-readable by the IWS CPU; writing to the EPROM is meaningless.

Display Planes

Display planes 1 and 2 at 8000:0h and 9000:0h, respectively, each contain 64 kilobytes of video pixel (bit-map) information making up the complete graphic image displayed. Since there are two display planes, software can select between the two, allowing one plane to be updated while the other is being displayed. The planes are selected by means of the Y9+ bit in the Control Register: when Y9+ is low, Plane 1 is displayed on the video display and when Y9+ is high, Plane 2 is displayed. Figure 2-4 below shows the address organization of the two display planes.

Each display plane consists of a 1024 by 512 rectangular linear array of bits that map into pixels on the video display. The visible area of the screen is a 656 by 510 bit map of the display plane. The origin of the visible screen has a fixed offset into the display plane, as shown in Figure 2-4.

For example, the first visible horizontal line (or bit map) starts at byte 8008:14h and ends at byte 8FF0:65h. Also, the first pixel shifted out to the video display is always the least significant bit of a byte. Therefore 8008:14h bit 0 is at the top left corner of the video

display and 8FF0:65h bit 7 is at the lower right. When programming, the nineteenth and twentieth bytes on each horizontal line should be set to 0 so that no extraneous dots appear on the video display. The two bytes immediately following the 82 bytes in each visible line should also be set to 0.

The display memory can be accessed by both the local CPU and the IWS CPU. The display memory controller provides a dual port for CPU and refresh accesses. This causes display memory accesses to be slower; the local CPU cycles can have five te selected by means of the Y9+ bit in the Control Register: when Y9+ is low, Plane 1 is displayed on the video display and when Y9+ is high, Plane 2 is displayed. Figure 2-4 below shows the address organization of the two display planes.

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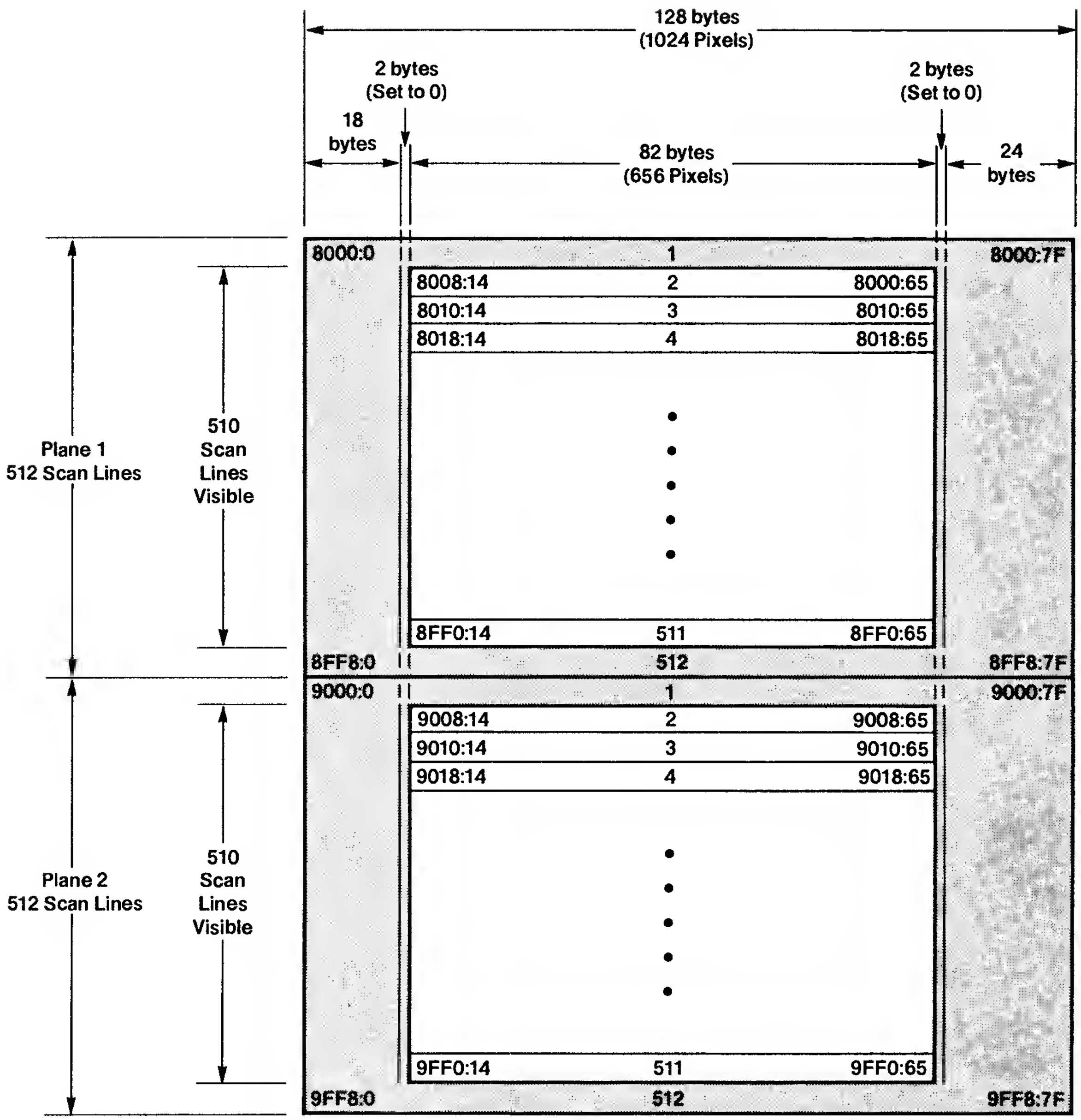
The display memory can be accessed by both the local CPU and the IWS CPU. The display memory controller provides a dual port for CPU and refresh accesses. This causes display memory accesses to be slower; the local CPU cycles can have five to 15 wait states (the average is 10) per access. Multibus cycles are even longer depending on the Multibus acquisition time. The display memory is byte-addressable locally but only word-addressable from the IWS CPU via the Multibus.



(Addresses are Hexadecimal)

Figure 2-4. Display Address Map.

THEORY OF OPERATION

This section addresses the needs of the engineer who must understand the IWS Graphics Control Board at a component level. Each of the functional blocks in Figure 3-1, IWS Graphics Control Board Block Diagram, is discussed in relation to the logic that performs the function.

The IWS Graphics Control Board is installed in one of the Multibus slots provided in the IWS workstation. It contains its own 8-MHz 8086-2 microprocessor, which considerably reduces the processing time required to generate a graphic image on the video display. The 8086-2 CPU operates from a program stored in 8 kilobytes of EPROM and stores data structures in 8 kilobytes of high speed RAM. Access by the CPU to both EPROM and RAM are made without wait states.

The CPU also writes to and reads from the 128-kilobyte display RAM array, which contains the video display information. The display RAM array is controlled by a synchronous display memory controller. This allows access, in one period of 1.25 microseconds, to the RAM array by either the 8086-2 CPU or IWS CPU and also provides video and display RAM refresh.

The memory controller is synchonized by a phase-locked loop providing a constant 26-MHz pixel clock, independent of the input pixel clock frequency (either 31 or 52 MHz) received from the IWS Video Board.

During a 1.25 microsecond display period, two 16-bit words of video information from the display RAM are serially shifted to the Video Board from the 32-bit video shift register.

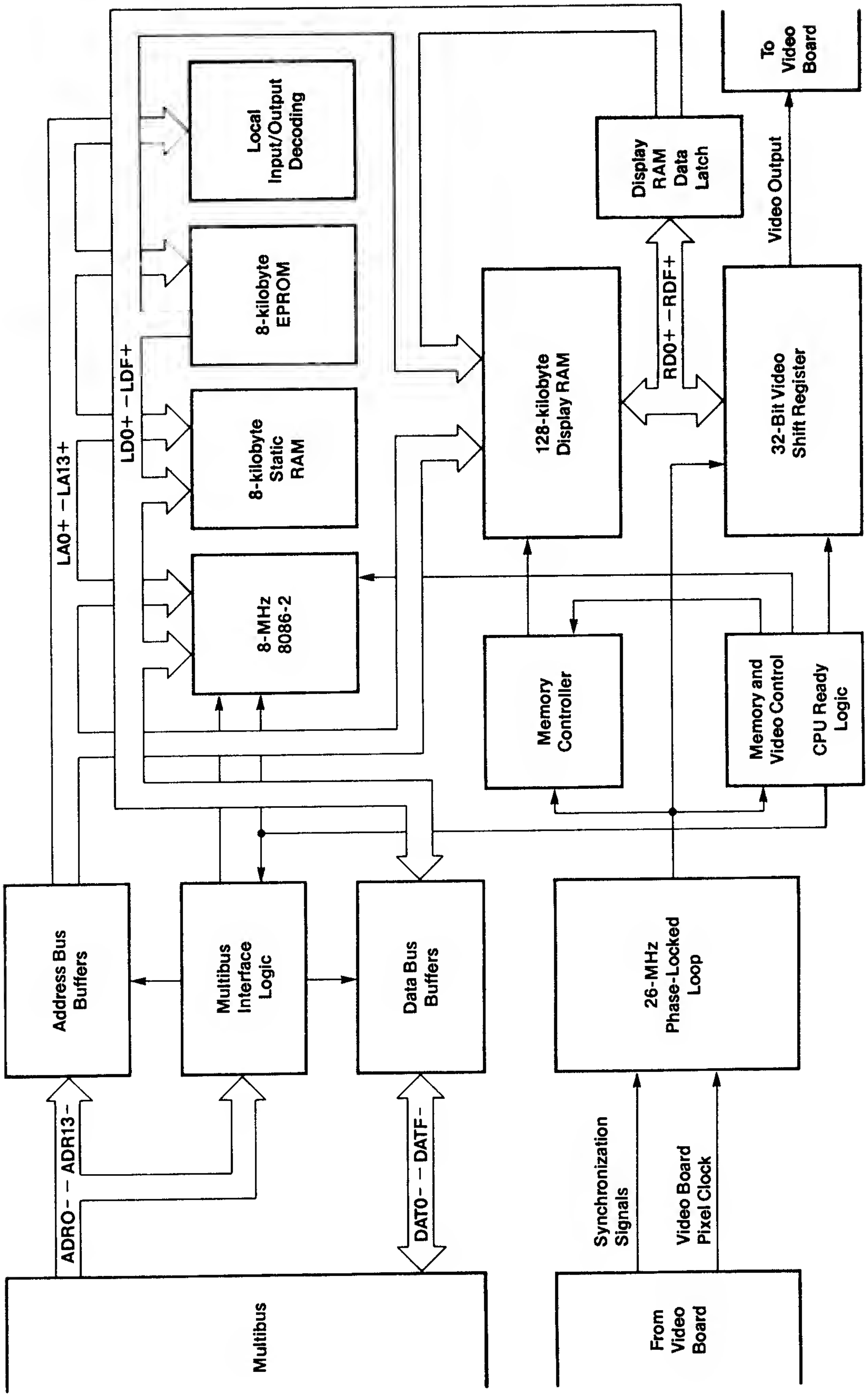


Figure 3-1. IWS Graphics Control Board Block Diagram.

Multibus Interface Logic

The IWS CPU communicates with the Graphics Control Board through the Multibus interface logic as shown below on page 6 of the IWS Graphics Control Board Schematic, Figure 3-2.

Local Address Bus

Address lines ADR0- through ADRF- are buffered from the Multibus by tri-state inverting drivers 9E and 8E and become LA0+-LAF+ (Local Address). The two drivers are enabled by SLAVE- at pins 1 and 19 when the Graphics Control Board is addressed by the IWS CPU.

Local Data Bus

Data lines DAT0- through DATF- are buffered to and from the LD0+-LDF+ (Local Data) by two inverting tranceivers, 11E and 10E. As with the address buffers, the two data tranceivers are enabled at pin 19 by SLAVE-. The direction of the data tranceiver's operation is determined by the MRDC- (Memory Read) command strobe from the Multibus.

Extended Address Register

An Extended Address Register at latch 12E supplies a low LBHEN- (Local Bus High Enable) to the display memory along with four additional high-order address lines: LA10+-LA13+ from the DAT0- through DAT3- lines at 12E's D-inputs. Latch 12E is also enabled by SLAVE- during a Multibus input/output cycle and clocked when port address comparator 7E detects a match between the four settings of DIP switch SW1 and the ADR0- through ADR7- address lines from the IWS CPU. (The port address values for SW1 are given in Table 2-2 in the "Architecture" section above.) Comparator 7E is enabled by the IOWC- (Input/Output Write Command) strobe from the Multibus. When a match occurs, pin 19 of 7E goes low to clock 12E and also generates a XACK- (Transfer Acknowledge) signal back to the Multibus through pin 6 of inverter 5D and pin 6 of gate 4E.

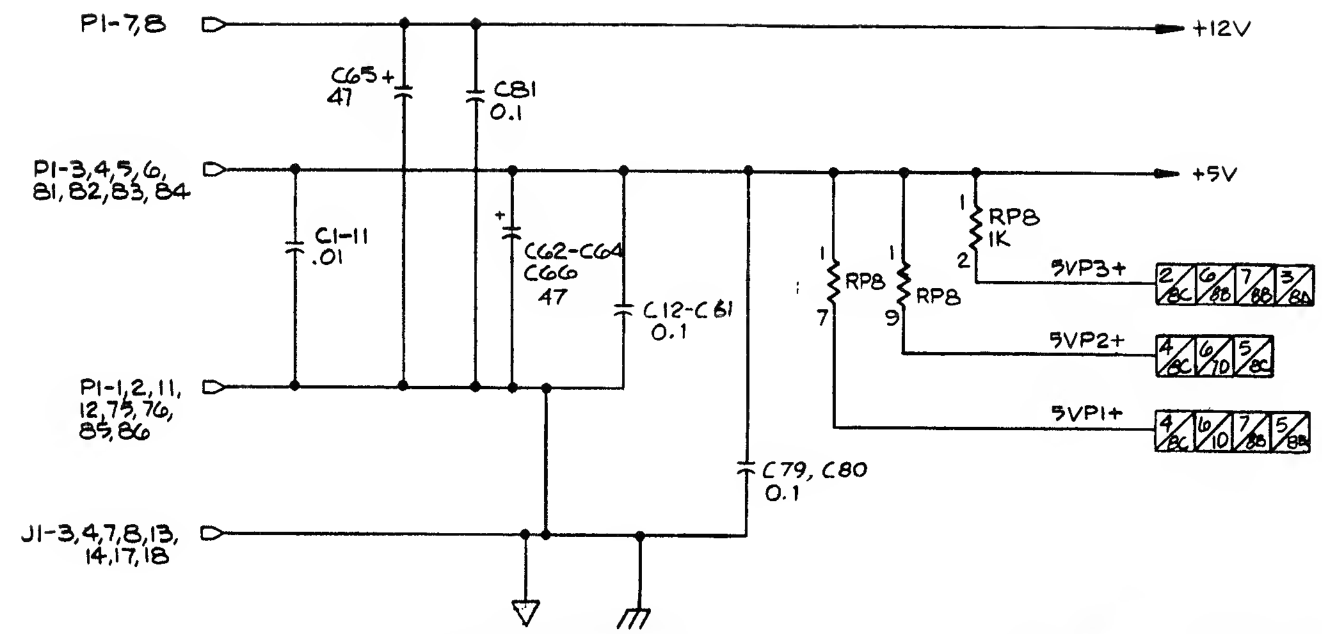
NOTES: UNLESS OTHERWISE SPECIFIED:

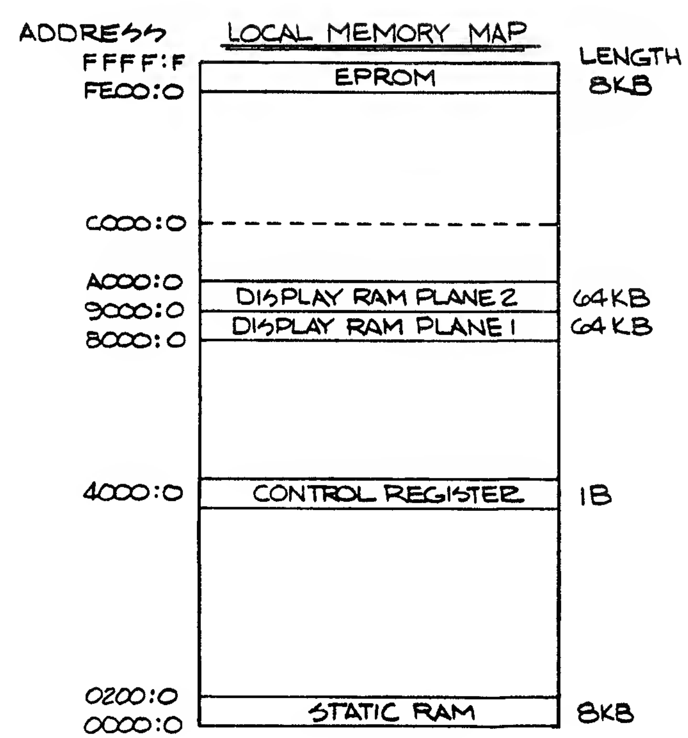
1. RESISTANCE VALUES ARE IN OHMS, 1/4W 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 7 & 14, 8 & 16, 10 & 20, 12 & 24, GROUND & POWER CONNECTIONS.
4. USED WITH ASSY. A-60-00068-00.

SPARE GATES		
TYPE	REF. DESIGNATORS	QTY
74LS374	12E	3
74LS244	2E	4
74S374	9B	1
10131	1A,	1
10104	6B	1
74LS393	12A	1
74LS373	18D	3
74S00	12C	1
74S02	9A	1
74S04	21C	2
74S22	5E	1
LM358	3B	1

REF. DESIGNATORS	
LAST USED	NOT USED
VR 1	
RP9	
C82	C 76
R24	
L1	
SW2	
Y1	
J1	
CR1	
Q8	

POWER AND GROUND LOCAION CHART					
REF. DES	TYPE	GND	+5V	+12V	
1A, 5A	10131	8	1,16		
6B	10104	8	1,16		
3A	10116	8	1,16		
7A, 1C	10137	8	1,16		
3B	LM358	4	—	8	
2B	1658	8	1,5		
6A	10102	8	1,16		





PORT SELECTION

SW1				OUTPUT PORT (HEX)
1	2	3	4	
OFF	OFF	OFF	OFF	XXØØ
OFF	OFF	OFF	ON	XX1Ø
OFF	OFF	ON	OFF	XX2Ø
OFF	OFF	ON	ON	XX3Ø
OFF	ON	OFF	OFF	XX4Ø
OFF	ON	OFF	ON	XX5Ø
OFF	ON	ON	OFF	XX6Ø
OFF	ON	ON	ON	XX7Ø
ON	OFF	OFF	OFF	XXØ1
ON	OFF	OFF	ON	XX11
ON	OFF	ON	OFF	XX21
ON	OFF	ON	ON	XX31
ON	ON	OFF	OFF	XX41
ON	ON	OFF	ON	XX51
ON	ON	ON	OFF	XX61
ON	ON	ON	ON	XX71

MULTIBUS MEMORY SELECTION

SW2				MEMORY RANGE (HEX)
1	2	3	4	
OFF	OFF	OFF	OFF	ØØØØ:Ø-ØFFF:F
OFF	OFF	OFF	ON	1ØØØ:Ø-1FFF:F
OFF	OFF	ON	OFF	2ØØØ:Ø-2FFF:F
OFF	OFF	ON	ON	3ØØØ:Ø-3FFF:F
OFF	ON	OFF	OFF	4ØØØ:Ø-4FFF:F
OFF	ON	OFF	ON	5ØØØ:Ø-5FFF:F
OFF	ON	ON	OFF	6ØØØ:Ø-6FFF:F
OFF	ON	ON	ON	7ØØØ:Ø-7FFF:F
ON	OFF	OFF	OFF	8ØØØ:Ø-8FFF:F
ON	OFF	OFF	ON	9ØØØ:Ø-9FFF:F
ON	OFF	ON	OFF	AØØØ:Ø-AFFF:F
ON	OFF	ON	ON	BØØØ:Ø-BFFF:F
ON	ON	DFF	OFF	CØØØ:Ø-CFFF:F
ON	ON	OFF	ON	DØØØ:Ø-DFFF:F
ON	ON	ON	OFF	EØØØ:Ø-EFFF:F
ON	ON	ON	ON	FØØØ:Ø-FFFF:F

Figure 3-2. IWS Graphics Control Board Schematic. (Page 1 of 7)

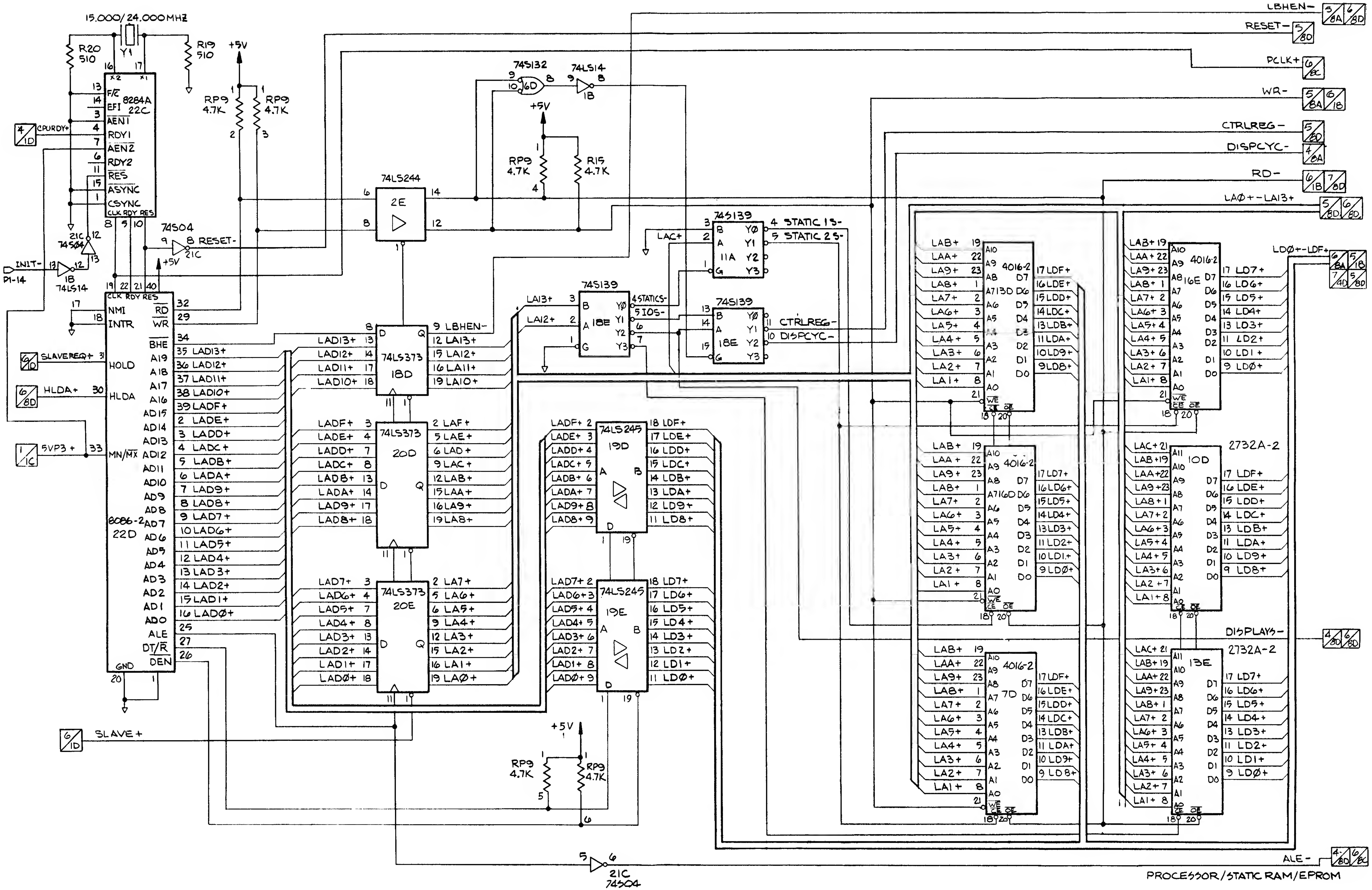


Figure 3-2. IWS Graphics Control Board Schematic. (Page 2 of 7)

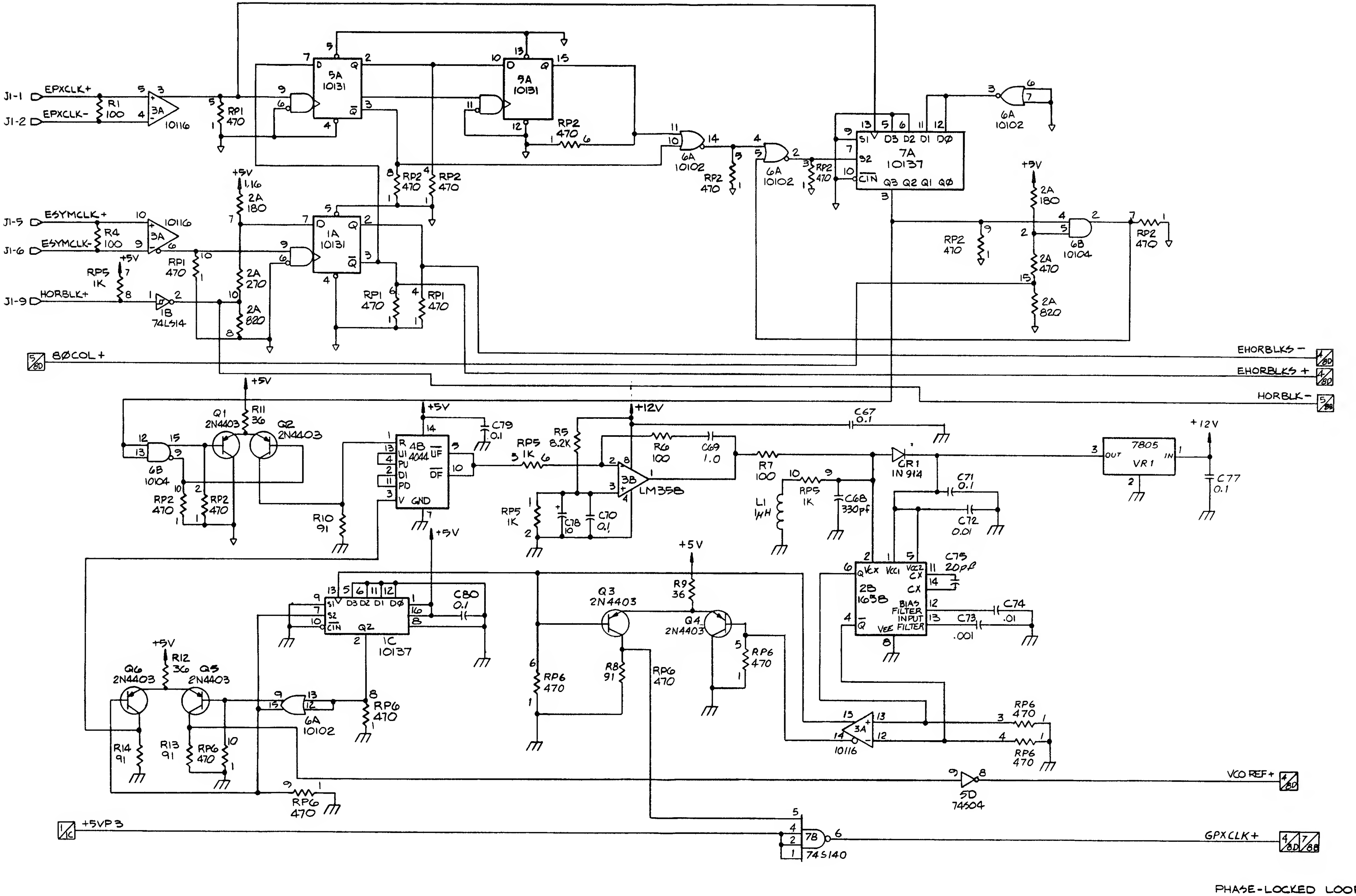


Figure 3-2. IWS Graphics Control Board Schematic. (Page 3 of 7)

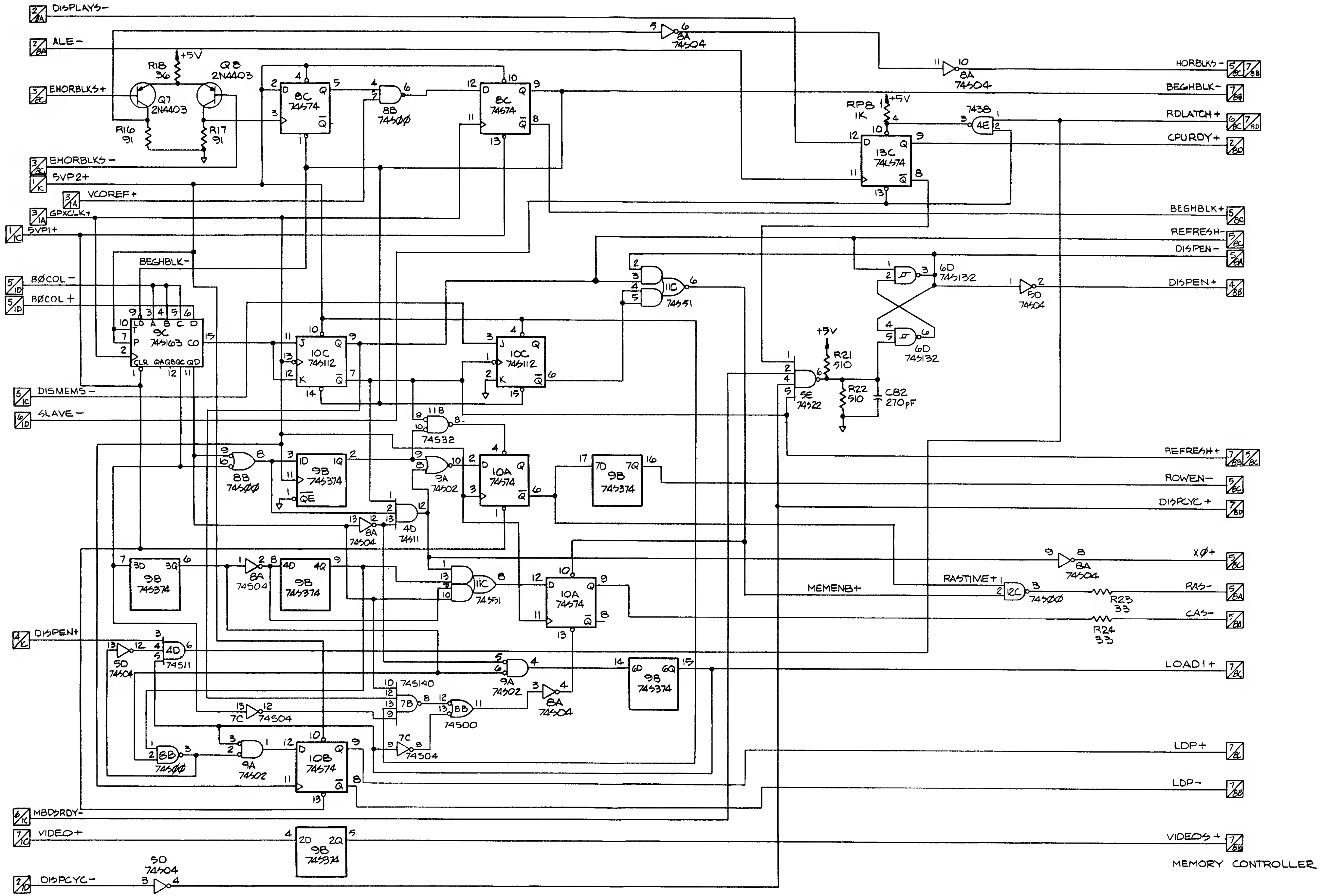


Figure 3-2. IWS Graphics Control Board Schematic. (Page 4 of 7)

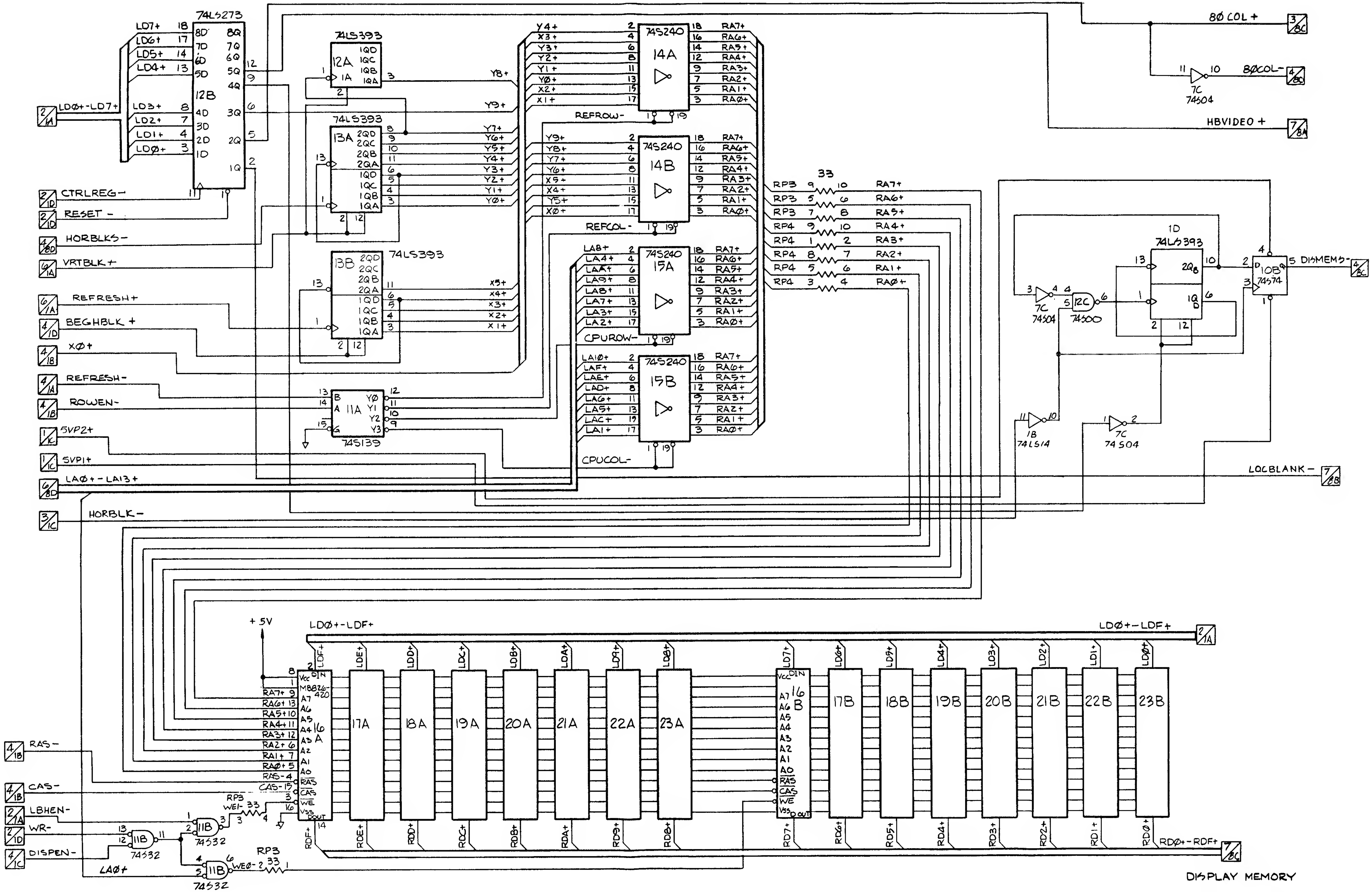


Figure 3-2. IWS Graphics Control Board Schematic. (Page 5 of 7)

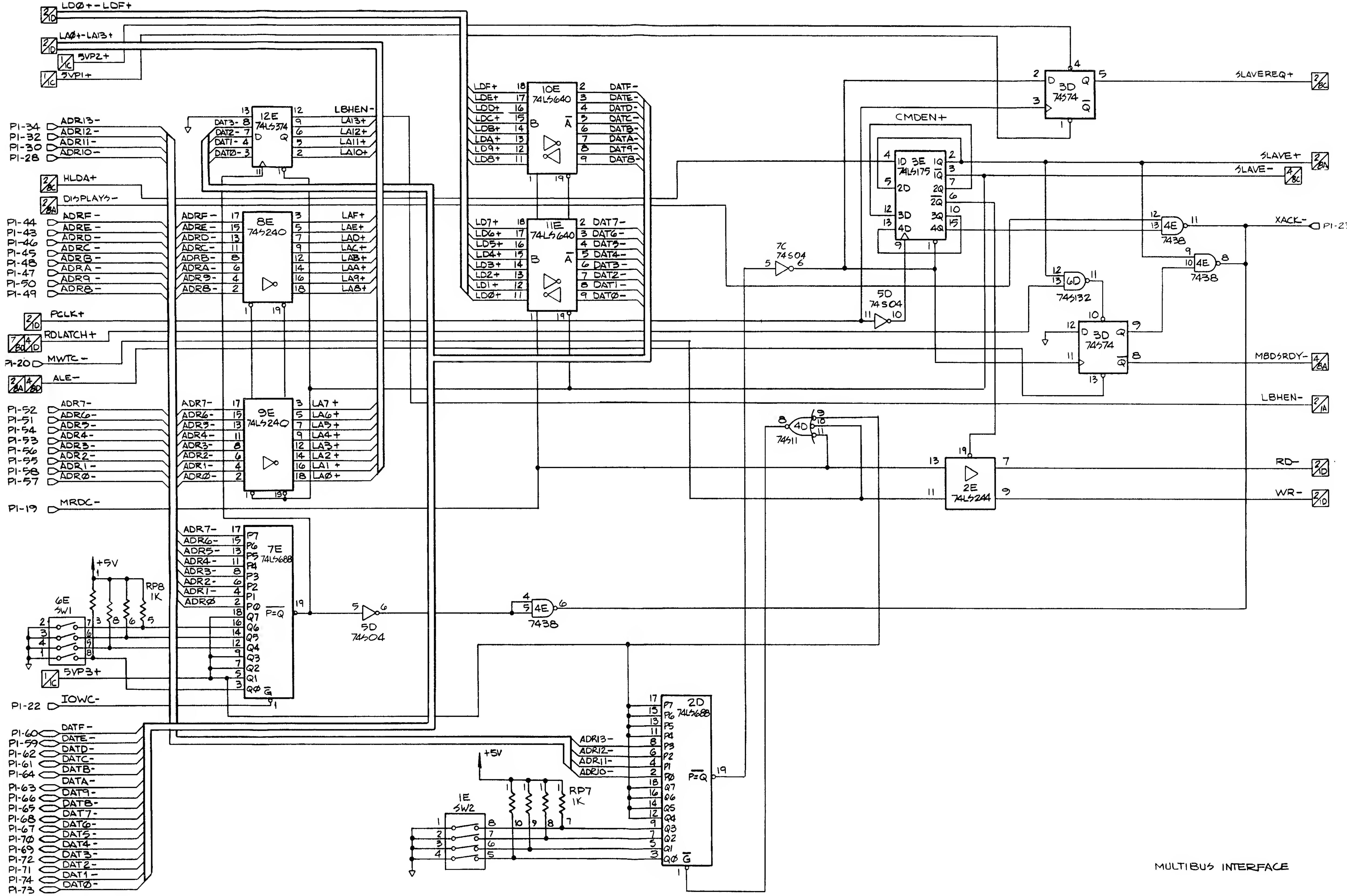


Figure 3-2. IWS Graphics Control Board Schematic. (Page 6 of 7)

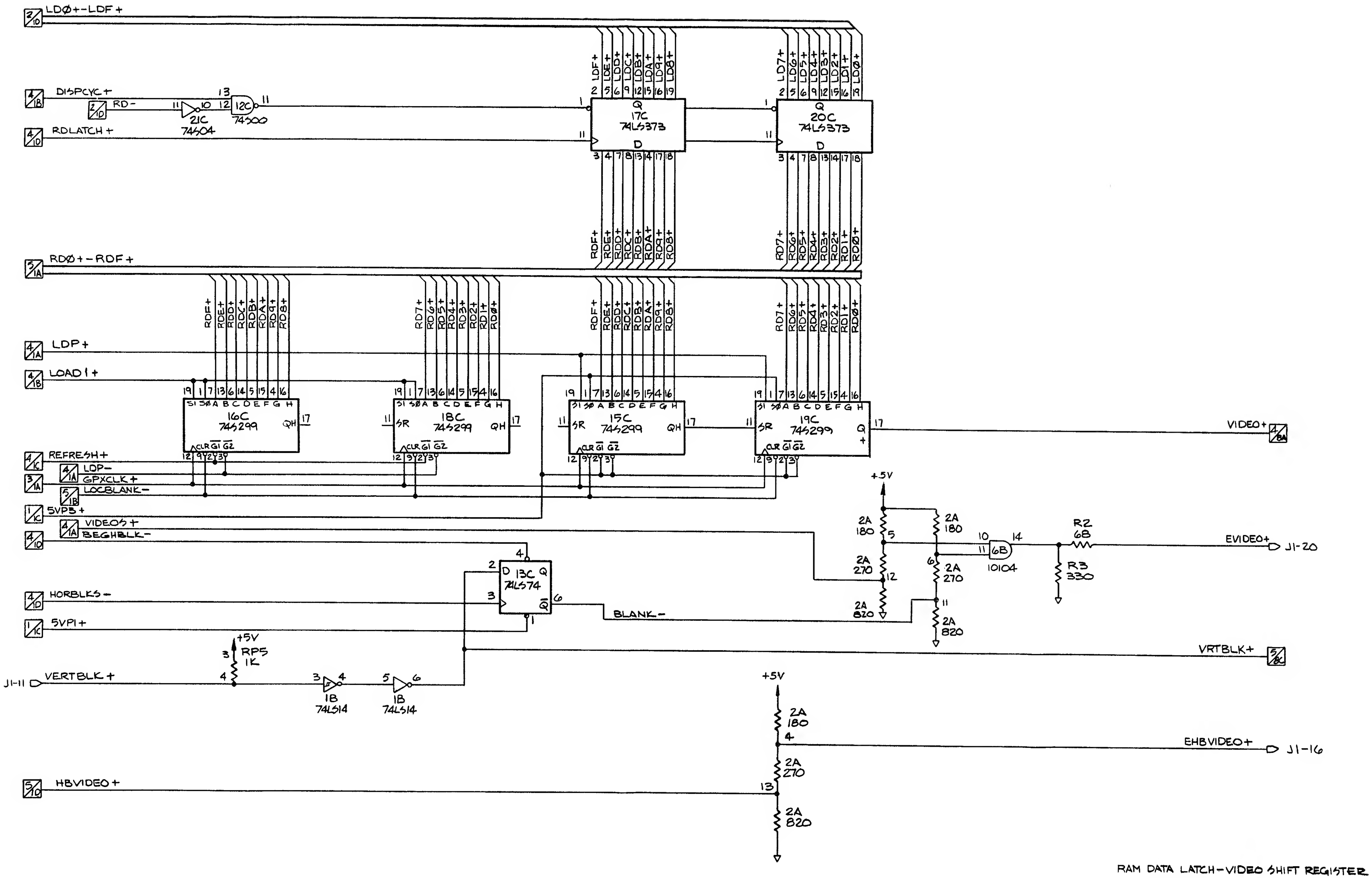


Figure 3-2. IWS Graphics Control Board Schematic. (Page 7 of 7)

Multibus Access

A multibus write or read cycle, to or from the local memory space, starts when the IWS CPU addresses the Graphics Control Board. Comparator 2D compares the incomming address on the four most significant address lines, ADR10- through ADR13- with the four settings of the SW2 DIP switch at 1E. The switch settings encode a single 64-kilobyte address segment out of the 1 megabyte of Multibus address space available. (The memory address values for SW2 are given in Table 2-1 in the "Architecture" section above.) Pin 19 of 2D goes low when the address matchs the switch settings at 2D's Q0-Q3 inputs and either the MWTC- (Memory Write) or MRDC- (Memory Read) command lines from the IWS CPU are low through pin 8 of gate 4D. The low at pin 19 of 2D is inverted to a high through pin 6 of inverter 7C.

The Multibus request at pin 6 of inverter 7C is synchronized to the processor clock PCLK+ at the D input of flip-flop 3D at pin 2. The output of pin 5, SLAVEREQ+ (Slave Request) is sent, as shown on page 2 of Figure 3-2, to the HOLD+ (Hold Request) input pin 31 of 8086-2 at 22D.

The high at pin 6 of 7C also clears the four D flip-flops at 3E, which are used to generate several control lines for a Multibus memory cycle. When the 8086-2 at 22D floats the local bus as requested by SLAVEREQ+, it asserts HLDA+ (Hold Acknowledge), which is sent to the 1D input of 3E at pin 4. After a positive transition of PCLK+, SLAVE+ (pin 2 of 3E) and SLAVE- (at pin 3 of 3E) are generated to enable the address and data drivers for a transfer from the Multibus to the IWS bus. One PCLK+ cycle later, the 2Q output of 3E at pin 6 goes low to gate 2E which buffers the MRDC- and MWTC- command lines to the RD- and WR- command lines used on the Graphics Control Board. The 2Q output of 3E at pin 6 is sent to the 3D input of 3E at pin 12 as CMDEN+ (Command Enable). After two more clock cycles, a high appears at the 4Q output of 3E to pin 13 of gate 4E. If DISPLAYS- (Display Cycle Select) is high, then nondisplay cycle resources (static RAM, EPROM, or the Control Register) are accessed. The timing produced at pin 13 of 4E generates XACK- (Transfer Acknowledge) at pin 11, indicating to the IWS CPU that the data on the data bus is valid.

If the display RAM is addressed (DISPLSYS- is low), XACK- originates at pin 8 of gate 4E. Pin 11 of flip-flop 3D is clocked by the high from pin 6 of inverter 7C. The Q output of 3D at pin 9 is low to pin 10 of gate 4E, which then disallows a XACK- to occur. When the data is valid on the data bus, pin 10 of 3D goes low from the NAND of SLAVE+ and RDLATCH+ at pins 12 and 13 of gate 6D, cause pin 9 of 3D to go high to pin 10 of 4E. Since pin 9 of 4E is also SLAVE+, XACK- appears at pin 8 of 4E. The Q- output of 3D at pin 8 goes low to generate MBDSRDY- (Multibus Display Ready), which is sent to the display memory controller described below. Finally, on the next processor cycle, pin 13 of 3D is cleared by ALE- from the 8086-2, thus making 3D's Q and Q- outputs false.

8086-2 Microprocessor, Static RAM, and EPROM Logic

As shown on page 2 of Figure 3-2 above, the Intel 8086-2 microprocessor at 22D executes instructions at 8 MHz and performs many control fuctions that would otherwise have to be handled by the IWS CPU. At pin 33, the 22D is strapped to operate in the minimum mode so the 8086-2's control lines operate in a manner similar to that of the Intel 8085 microprocessor. The 8086-2's HOLD+ input at pin 31 is used by SLAVEREQ+ (Slave Request) from the Multibus interface logic. SLAVEREQ+ requests that the 8086-2 isolate itself from the address and data busses so that the IWS CPU can use them. When the 8086-2 has complied with the request, it sets its pin 30 HLDA+ line high to the Multibus interface. Also, since the 8086-2 is not interrupted by any external device, the INTR+ (Interrupt) and NMI+ (Nonmaskable Interrupt) inputs are both tied to ground. The 8086-2's RD- (Read) and WR- (Write) command lines are buffered at pins 14 and 12 of 2E, respectively, and control the action to other circuits on the board.

Local Address Bus

The 8086-2's LAD0+-LAD13+ (Local Address and Data) lines are sent through address latches 20E, 20D, and 18D to hold a memory address for the duration of a memory cycle, since the LAD bus is multiplexed with data. When ALE+ at pin 25 of 22D goes low during a local read or write cycle,

the address is latched. The outputs of 20E, 20D, and 18D are LA0+-LA13+ (Local Address) and are enabled only when SLAVE+ is low, meaning that the IWS CPU does not control the local address bus. Also latched at 18D is LBHEN- (Local Bus High Enable). When low, LBHEN- enables data onto the eight most significant data lines, LD8+-LDF+; otherwise, data is placed on the LD0+-LD7+ data lines.

Local Data Bus

Data transceivers 19E and 19D are used to buffer the LAD0+-LADF+ data and address lines to the LD0+-LDF+ (Local Data) lines. Two signals from the 8086-2 control 19E and 19D: DEN- (Data Enable), which enables the transceivers during a read or write cycle and DT+/R- (Data Transmit or Receive), which sets the direction of the transceivers. When DT+/R- is high, data flows from the LAD bus to the LD bus.

Clock, Reset, and Ready Logic

The clock, reset, and ready logic are provided by an Intel 8284A clock generator at 22C run by a 24.000-MHz crystal, Y1. The 8284A divides the crystal frequency by three to make an 8-MHz processor clock. The 8284A also supplies a RDY+ (Ready) signal to the 8086-2, which is synchronized to the processor clock. The asynchronous ready input signal to the 8284A is CPURDY+ and is used to signal the 8086-2 that it can access the on-board display memory. The master reset for the Graphics Control Board comes from pin 14 of the P1 Multibus connector as INIT- (Initialize) and is synchronized to the processor clock as RES+ (Reset). RES+ is sent to pin 21 of the 8086-2 and is inverted at pin 8 of 21C as RESET- to clear the Control Register (see page 5 of the Figure 3-2).

Input/Output Decoding

Input/Output Decoders 18E and 11A decode various memory-mapped input/output type selection lines for the Graphics Control Board. Based on the condition of the two most significant local address lines, LA12+ and LA13+, 18E decodes four input/output 256-kilobyte address segments. The four address segements are:

- STATICS- (Static RAM Select) at pin 4 of 18E. STATICS- gates pin 1 of decoder 11A to select one of two 4-kilobyte segments of static RAM. Local address line LAC+ selects one or the other at pin 2 of 11A. The outputs of decoder 11A are STATIC1S- (Static RAM 1 Select) at pin 4 and STATIC2S- (Static RAM 2 Select) at pin 5.

- IOS- (Input/Output Select) at pin 5 of 18E. IOS- is sent to the B input of 18E at pin 13 to cause 18E's Y1 output at pin 11 to go low as CTRLREG- (Control Register). The Control Register at 12B (see page 5 of Figure 3-2) provides five control bits selected by the graphics software. (The Control Register is described in the "Architecture" section above.) Pin 15 of 18E (see page 2 of Figure 3-2) must be gated by a read or write command strobe through pin 8 of inverter 1B and pin 8 of gate 6D. Note that, even though the read command strobe can be used in this case to gate 18E, the Control Register can only be written to. A read command alters the Control Register to an indeterminate state.

- DISPLAYS- (Display Select) at pin 6 of 18E. DISPLAYS- is sent to the B input of 18E at pin 14. The Y2 output of 18E at pin 10, DISPCYC- (Display Cycle), selects the display RAM for a read or write. Again, pin 15 of 18E must be gated by a read or write command strobe. DISPLAYS- is also sent to the CPURDY+ (CPU Ready) flip-flop (see page 4 of Figure 3-2) and the Multibus Interface Logic (page 6 Figure 3-2).

- EPROM at pin 7 of 18E. EPROM is enabled at 10D and 13E by pin 7 of 18E when high addresses are decoded.

Static RAM

The 200-ns 4116-2 static RAMs at 7D, 13D, 16D, and 16E provide 8 kilobytes of data storage for the 8086-2. At the pin 18, CE- (Chip Enable) inputs to the RAMs, 16D and 13D are enabled by STATIC1S-; 16E and 7D are enabled by STATIC2S-. When enabled, each of the RAMs are written to, using the WR- command strobe at the pin 21 WE- (Writer Enable) input. During a read operation, the outputs of each RAM are enabled using the RD- command strobe at pin 20. RAMs 16D and 16E are read from, and written to, on the LD0+-LD7+ data lines; 13D and 7D are read from, and written to, data on the LD8+-LDF+ data lines. All of the RAMs are addressed using the LA1+-LAB+ local address lines.

Firmware EPROM

Eight kilobytes of firmware for the 8086-2 is stored in two 200-ns 2732A-2 EPROMs at 13E and 10D. The EPROMs are addressed through the LA1+-LAC+ local address lines; EPROM 13E places data on the LD0+-LD7+ during a read cycle and 10D places data on the LD8+-LDF+ data lines. The EPROMs are each selected at pin 18; the outputs are enabled at pin 20.

26-MHz Phase-Locked Loop

The phase-locked loop fundamentally performs two basic functions on the Graphics Control Board:

- The phase-locked loop synthesizes a 26-MHz pixel clock from the 31- or 52-MHz pixel clock supplied by the IWS Video Board. A constant 26-MHz clock ensures that the graphics image on the video display is independent of the 80 or 132 column alphanumeric mode being used.

- The phase-locked loop synchronizes the graphics display to the alphanumeric display. That is, the phase-locked loop ensures that the Graphics Control Board circuitry is synchronized to the horizontal and vertical synchronization signals from the Video Board in the IWS.

In the 80-column alphanumeric mode, the Video Control Board provides a 31.185-MHz pixel clock to the phase-locked loop. To synthesize a 25.988-MHz pixel clock, the phase-locked loop multiplies the input pixel clock by five-sixths. In the 132-column alphanumeric mode, the input pixel-clock frequency is 51.975 MHz. To arrive at 25.988 MHz, the phase-locked loop divides the input pixel clock by two. A block diagram of the 26-MHz phase-locked loop is shown in Figure 3-3 below.

As shown above on page 3 of Figure 3-2 (IWS Graphics Control Board Schematic), ESYMCLK+ and ESYMCLK- (ECL Symbol Clock) are balanced differential input signals to line receiver 3A at pins 9 and 10, respectively. Originating on the the Video Control Board, ESYMCLK+ and ESYMCLK- have a 20% duty cycle and run at one-tenth the frequency of the input pixel clock. The symbol clock signals the beginning of each symbol or character on the video display in either the 80- or 132-character alphanumeric mode.

The symbol clock output at pin 6 of 3A clocks synchronizing flop-flop 1A at pin 9. The D input of 1A at pin 7 is HORBLK+ (Horizontal Blank). HORBLK+ is a 31.5-kHz blanking signal from the Video Board that is inverted at pin 2 of 1B. It is then converted from standard TTL levels to ECL levels by a voltage divider composed of 820-, 270-, and 180-ohm resistors at 2A. The Q and Q- outputs of flip-flop 1A generate complementary synchronized horizontal blank signals as EHORBLKS- (Synchronized ECL Horizontal Blank) and EHORBLKS+, respectively, which are used to disable video output during the time when the video beam is horizontally retracing the screen to start a new scan line. From the Q- output of 1A, EHORBLKS+ is also sent to the D input at flip-flop 5A to be synchronized with the incoming EPXCLK+ (ECL Pixel Clock) and EPXCLK- from pin 3 of differential line receiver 3A. The Q output of 5A at pin 2 is connected to the D input of 5A at pin 10 to be synchronized again with the next pixel clock. The flip-flops at 5A generate one 39-ns, positive-going pulse at pin 14 of NOR gate 6A. This preload pulse is used to set the S2 mode input on decade counter 7A. The preload pulse indicates that a new horizontal scan line has begun at the first pixel of the first character on a new horizontal scan line.

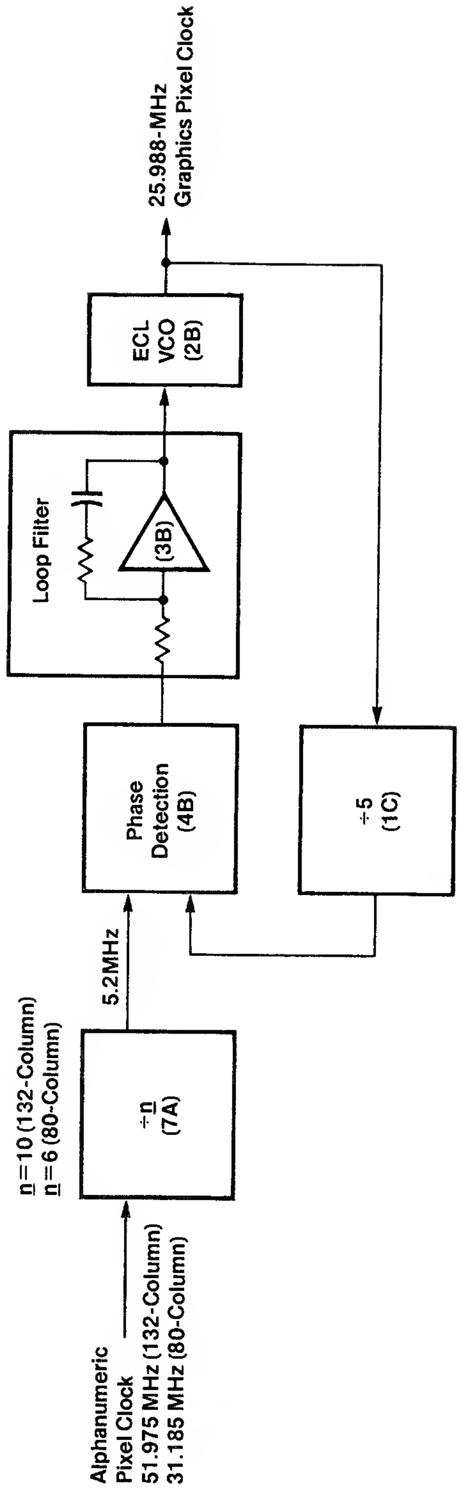


Figure 3-3. 26-MHz Phase-Locked Loop Block Diagram.

When the synchronized horizontal blank signal is clocked to the D input of 5A at pin 7, the Q-output at pin 3 goes low to pin 10 of gate 6A. During this time, pin 11 of 6A is low, causing a high at pin 14. This starts the preload pulse. Since the high at pin 2 of 5A is sent to the D input of 5A at pin 10 (and keeping in mind that both flop-flops at 5A are clocked together), the next pixel clock cycle clocks a high through pin 15 of 5A to pin 11 of gate 6A. The high at pin 11 causes pin 14 of 6A to go low, thus ending the preload pulse after 39 ns. The preload pulse is sent through pin 14 of gate 6A to pin 4, inverted at pin 2 of 6A, and sent to counter 7A's S2 mode input at pin 7.

Counter 7A is a divide-by-n counter that generates a 5.2-MHz VCO (Voltage-Controlled Oscillator) reference signal at its Q3 output, regardless of the alpanumeric mode being used. When 7A's S2 input goes high, the counter loads a three from its high pin 11 and 12 D-inputs and then starts to increment. The clock for 7A is the pixel clock from pin 3 of receiver 3A. From the initial counter preload of three, 7A divides the 51.975-MHz input pixel-clock frequency by 10 in the 132-column alphanumeric mode, using the Q3 output at pin 3. Counter 7A continues to divide the pixel clocks by 10 (5.2 MHz) until the next scan line causes 7A to preload a three, 1650 pixel clocks later.

If the 80COL+ (80-Column Mode) line from pin 5 of the the Control Register (see page 5 of Figure 3-2) is high, counter 7A divides the pixel clocks by six until the next horizontal scan line occurs. 80COL+ is converted from a TTL level to an ECL level by the 820-, 470-, and 180-ohm resistor voltage divider at pin 2 of resistor pack 2A. The high ECL level is sent to pin 5 of gate 6B where it is ANDed with 7A's Q3 output at pin 2. Pin 2 of 6B goes high to pin 5 of 6A causing a preload of three at 7A. Counter 7A increments until its Q3 output goes high again, for a total of six counts. As long as 80COL+ is high, 7A will only count to eight before it is preloaded to three again. The Q3 output divides the 80-column mode 31.185-MHz pixel clock by six to a 5.2-MHz VCO reference signal, which is sent to an ECL-to-TTL converter at pins 12 and 13 of gate 6B and transistors Q1 and Q2.

When pins 12 and 13 of 6B are high, pin 9 of 6B is low to the base of transistor Q2, thus turning

on Q2 and causing a high of about 2.5 V dc to appear at REF (Reference) input at pin 1 of the TTL phase detector circuit 4B. When pin 9 of 6B is high, the input to 4B is low. Phase detector 4B compares the phase of the 5.2-MHz reference signal at pin 1 of the VCO (Voltage-Controlled Oscillator) input at pin 3. A difference in phase between the VCO and the REF inputs results in a error voltage applied to the minus (-) input of charge pump 3B at pin 2. The reference voltage applied to 3B is determined by R5, and the resistor at pins 1 and 2 of RP5. R6 and C69 set the charge pump function of 3B. The reference voltage for 3B is about +1.3 V dc, which is approximately the center point between a TTL low level and a TTL high level. The output of 3B is sent through a 100-ohm series resistor at R7 to the input of VCO 2B at pin 2. The output of 3B is also affected by a filter made up of L1, a resistor at pins 9 and 10 of RP5, and C68 to reduce high frequency noise. Since 3B is supplied by +12 V dc to provide an adequate voltage swing and low noise, diode CR1 clamps the output of 3B to a maximum of 5.7 V dc to avoid damage to the VCO. The VCO changes its output frequency depending upon the voltage level at its pin 2 Vcx input. The complementary Q and Q- outputs of 2B at pins 4 and 5, respectively, are oscillating at 25.988 MHz when the phase-locked loop is locked to the incoming pixel clock.

The Q output of 2B is sent to the clock input of counter 1C, which divides the VCO reference signal by five (to 5.2 MHz) at its Q2 output at pin 2. The output is sent to gate 6A to provide both phases of the 5.2-MHz reference signal to an ECL-to-TTL converter made up of transistors Q5 and Q6. One phase of the TTL VCO reference signal from the collector of Q6 is sent to the pin 3 VCO input of phase detector 4B to be compared with the signal on the REF input at pin 1. The other phase of the TTL VCO reference signal, from the collector of Q5, is inverted at pin 8 of 5D and sent to the memory controller as VCOREF+ (Voltage-Controlled Oscillator Reference).

The ECL Q output of 2B is also converted to a TTL signal at the converter at Q3 and Q4. The reference signal is sent from the collector of Q3 to the pin 5 input of gate 7B. The other three inputs of 7B are tied to +5 V dc to minimize the input current required. Gate 7B provides a large

amount of current to drive the resulting inverted GPXCLK+ (Graphics Pixel Clock) to the memory controller.

Synchronous Display Memory Controller

The synchronous display memory controller allows access to the 16 64-kilobyte dynamic RAMs making up the display memory. The entire memory controller is synchronized on a line-by-line basis. If the video display loses its synchronization at any time, only the scan line currently being displayed is affected.

Display Memory Cycle Generation and Timing

The state machine generates all of the necessary control signals at the appropriate time to generate a display memory cycle. Each display memory cycle is divided into two 624-ns halves; each half is sixteen 39 ns pixel-clock states. The first half of the cycle is used by the memory controller to provide 32 pixels of video refresh as well as a row of dynamic RAM refresh; the second portion of the cycle allows read or write access to the display memory by a CPU.

The phase-locked loop described above provides most of the input signals used by the memory controller. As shown in the upper left corner of page 4 of Figure 3-2, both phases of the synchronized horizontal blank signal, EHORBLKS+ and EHORBLKS-, are sent to an ECL-to-TTL converter at transistors Q7 and Q8. The TTL horizontal-blank signal clocks flip-flop 8C pin 5 high to pin 4 of NAND gate 8B. At pin 5 of 8C, the 5.2-MHz VCOREF+ signal from the phase-locked loop gates the horizontal blank signal to pin 6 of 8C. The resulting low at pin 6 of 8C is sent to the D input of 8C at pin 12. On the next positive edge of GPXCLK+, 8C at pin 11, a low appears at pin 9 of 8C as BEGHBLK- (Begin Horizontal Blank). BEGHBLK- goes back to reset pin 1 of flip-flop 8C, causing BEGHBLK- to go low for a single pixel-clock period of 39 ns. BEGHBLK- is also sent to the video blanking flip-flop (see page 7 of Figure 3-2) as well as to the pin 9 LD (Load) input of counter 9C to synchronize the memory controller. BEGHBLK- is used to disable the display memory for part of an incomplete cycle.

BEGHBLK- occurs once for every horizontal scan line and causes counter 9C to preload either a seven or an eight depending on the alphanumeric mode being used. The 4-bit counter at 9C and flip-flop 10C pins 7 and 9 form a divide-by-32 (5-bit) counter to time the memory controller state machine, which creates the control signals used in the 32-state memory cycle. Counter 9C requires a preload to compensate for the fact that the number of pixel states in a horizontal scan line (825) is not evenly divisible by 32. During these 825 pixel-clock states, the state machine generates a total of 25 full 32-state memory cycles per scan line with a twenty-sixth incomplete cycle of 25 states.

Counter 9C divides the pin 2 GPXCLK+ input at its QC and QD outputs. The CO (Carry Out) output at pin 15 of 9C is sent to the J and K inputs of flip-flop 10C at pins 11 and 12, respectively. When clocked by GPXCLK+, flip-flop 10C pins 7 and 9 toggle every 16 GPXCLK+ cycles to divide the display memory cycle between refresh and processor read or write cycles. The Q output of 10C at pin 9 is REFRESH- (Refresh Cycle Active) indicating that the display memory cycle is in the refresh half.

The Q- output of 10C at pin 7 is used to clock pin 1 of 10C, which (through AND/OR gate 11C) disables the display memory during the incomplete twenty-sixth memory cycle or during a change between the 80- or 132-column alphanumeric modes. BEGHBLK- disables display memory during the twenty-sixth cycle by resetting flip-flop 10C at pin 15. A reset causes pin 6 of 10C to go high at pins 4 and 5 of gate 11C. A low results at pin 6 of 11C as MEMENB+. MEMENB+ is further gated with RASTIME+ (Row Address Synchronous Timing) from the state machine at pins 2 and 1 of gate 12C. The output at pin 3 of 12C is the RAS- (Row Address Strobe) to the dynamic RAM array. MEMENB+ also sets pin 10 of flip-flop 10A to disable CAS- (Column Address Strobe).

Another case of MEMENB+ operating to disable memory occurs when the graphics software switches from one alphanumeric mode to another. When the mode is switched, the phase-locked loop must have enough time to reaquire the 26-MHz pixel-clock frequency. During this time, the phase-locked loop is unstable and can cause the memory controller to mistime its memory access.

Circuitry shown on the right side of page 5 of Figure 3-2 consisting of counter 1D, flop-flop 10B, gate 12C, and inverters at 1B and 7C provides a signal to disable the memory controller for about 1 ms during a mode change. Bit 4 of Control Register 12B enables counter 1D just before the alphanumeric mode changes. When HORBLK- goes low, it clocks the pin 1 output of 1D along with the pin 3 clock input of flip-flop 10B. DISMEMS- (Disable Memory Synchronized) at pin 5 of 10B is sent to the J input of flop-flop 10C at pin 4 (see page 4 of Figure 3-2) When pin 1 of 10C is clocked, pin 6 of 10C goes low, thus disabling both RAS- at pin 2 of 12C and CAS- at pin 10 of flip-flop 10A. After a period of about 1 ms, DISMEMS- goes high again having given the phase-locked loop enough time to reaquire the pixel clock frequency. DISMEMS- only changes at the beginning of the horizontal blank period, insuring that memory strobes are not gated with incorrect timing.

State Machine and Display Memory

The memory controller state machine is composed of the latches, flip-flops, gates, and inverters shown on the bottom half of page 4 of Figure 3-2. For each of the 32 memory cycle states clocked by counter 9C and flip-flop 10C, the state machine sequentially enables and disables certain memory control lines, thus controlling the display memory cycle. The state machine works in conjunction with the logic on the top half of page 5 of Figure 3-2 to read from, write to, and refresh the 16 display RAMs on the bottom half of page 5 of Figure 3-2. In addition to pages 4 and 5 of the schematic (Figure 3-2), refer to Figure 3-4, Display Memory Refresh Timing Diagram during the following discussion.

In the display memory refresh cycle (states 0-15), REFRESH- (Refresh Cycle Active) from pin 9 of 10C goes low (page 4, Figure 3-2). REFRESH-, together with a low ROWEN- (Row Enable) from pin 16 of latch 9B, select the Y0 output of decoder 11A (see the the middle left area of page 5 of Figure 3-2) to gate the address of the refresh row from counters 13A and 13B through buffer 14A to the RA0+-RA7+ (Row Address) lines. At state 1, when the row address is stable on RA0+-RA7+, RAS- goes low from pin 3 of gate 12C to pin 4 on each of the 64-kilobyte dynamic RAMs. ROWEN-

then goes high (see page 5 of Figure 3-2), which selects the Y1 output of 11A. The refresh column buffer at 14B is selected to enable a refresh column address from counters 13B, 13A, and 12A onto the RA0+-RA7+ lines.

The refresh row and column addresses originate at counters 13B, 13A, and 12A. Counter 13B is cleared at pins 2 and 12 at the start of every horizontal scan line by the BEGHBLK+ pulse and is incremented when a refresh cycle occurs, as indicated by REFRESH+ going high. Counter 13B's X1+-X5+ (X-Axis Address) outputs are sent to buffers 14A and 14B to partially form the refresh row and column address. Counters 13A and 12A are both cleared at the end of every display screen by VRTBLK+ (Vertical Blank). Counter 13A is incremented by HORBLK- (Horizontal Blank) while 12A is incremented by the high-order output of 13A, Y7. The Y0+-Y8 (Y-Axis Address) outputs of 13A and 12A are arranged at the inputs to buffers 14A and 14B along with the X1+-X5+ address bits to allow the display RAM to be completely refreshed in as short a time as possible. Note that the row address buffer 14A, has the lowest-order X and Y bits of the address as its inputs. These low-order bits toggle most frequently while 13A, 12A, and 13B are counting and thus allow all 128 rows of memory in the display RAMs to be refreshed every 512 microseconds.

Buffer 14B contains the higher-order X and Y bits to form the column address. All but two of the inputs to 14B come from the refresh address counters: X0+ and Y9+. The low-order X0+ bit, from the state machine, changes state during every refresh cycle to generate two column addresses for two page-mode read cycles described below. The high-order Y9+ bit, from the Control Register, specifies one of the two viewports to be refreshed, as described in the "Architecture" section.

When a column address is on the RA0+-RA7+ lines, the CAS- (Column Address Strobe) from pin 9 of flip-flop 10A occurs at state 3. The X0+ bit from the state machine then goes high, causing the column address to increment at the RA0+ through RA7+ outputs of buffer 14B. Along with the second column address, a second CAS- pulse is issued from the state machine at state 10.

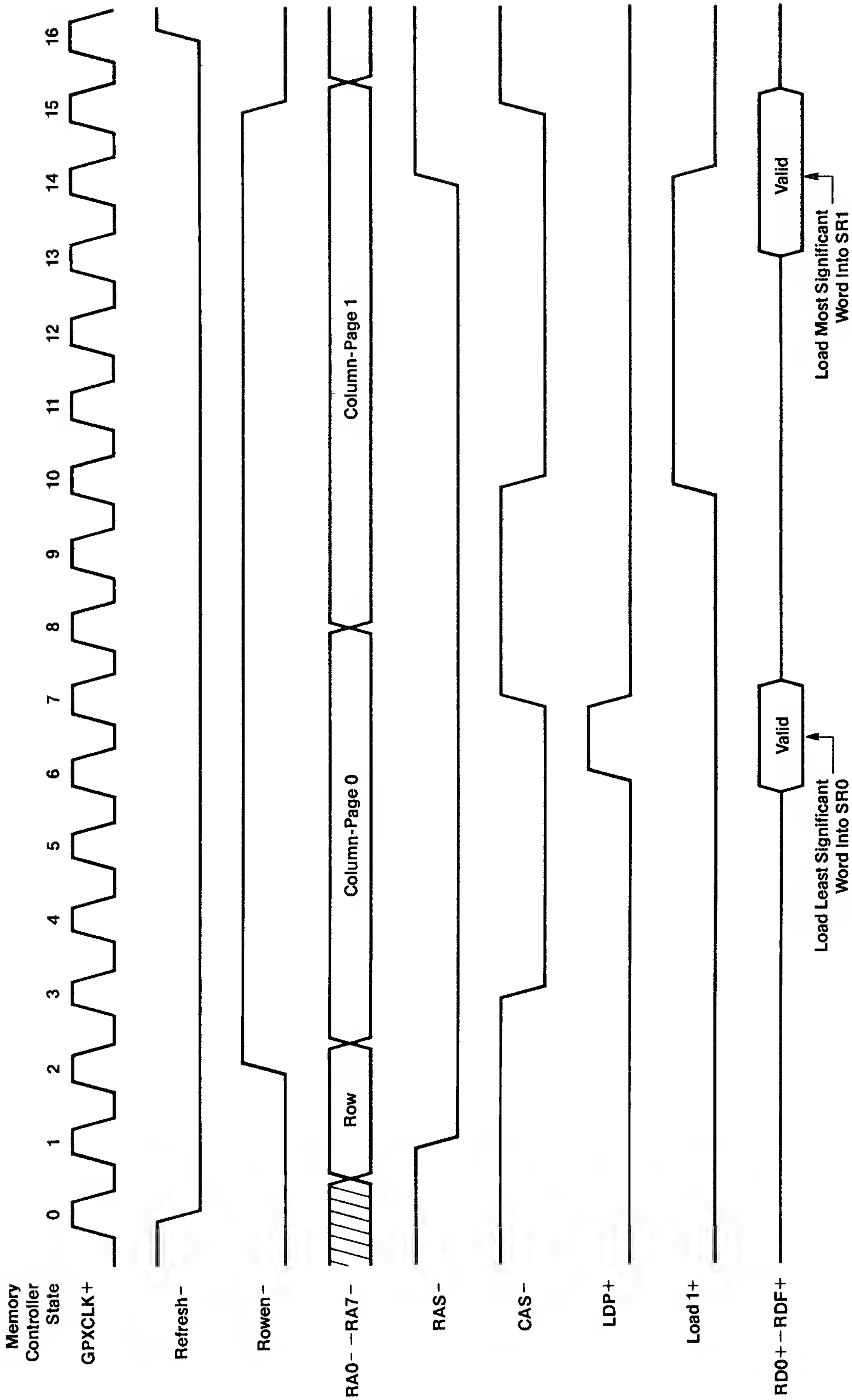


Figure 3-4. Display Memory Regresh Timing Diagram.

The two CAS- signals sent to the pin 15 inputs of the RAMs allow two pages of the display memory, 0 and 1, to be refreshed during a single cycle. For page 0, data first appears on the RD0+-RDF+ (RAM Data) lines at state 6. Since the refresh cycle is basically a RAM read cycle, the corresponding LDP+ (Load Pulse) from pin 9 of flip-flop 10B and the LOAD1+ (Load Shift Register 1) from pin 15 of 9B appear at states 6 and 10, respectively, to load and move data on the RD0+-RDF+ (RAM Data) lines to video shift registers described below under "RAM Data Latches and Video Shift Registers." Finally, at state 14, the state machine causes RAS- to go high and LOAD1+ to go low, thus ending the refresh cycle.

A display memory read cycle (states 16 through 32) has different timing than the refresh cycle. Since the row and column addresses originate at either the IWS CPU or Graphics Board CPU, the row and column counters are not used. Also, only one RAM-column address is generated. The timing of the cycle is shown in the Display Memory Access Timing Diagram, Figure 3-5 below. At state 16, the display memory starts with a low REFRESH+ from pin 7 of flip-flop 10C. REFRESH+, from the Q- output of 10C is the inverted form of REFRESH- used in the display memory refresh cycle described above. Since REFRESH- is high at this time and ROWEN- is low, CPUROW- (CPU Row Address) at the Y2 output of decoder 11A, is selected (as shown on page 5 of Figure 3-2). CPUROW- gates a row address on the LA2+, 3+, 4+, 7+, 8+, 9+, A+, and B+ local address lines to the corresponding RA0+-RA7+ RAM address line through buffer 15A to the display RAM's A0+-A7+ address inputs. At state 18, RAS- goes low to strobe the row address into the RAMs and at state 19, ROWEN- goes high, thus selecting CPUCOL- (CPU Column Address) at the Y3 output of decoder 11A. CPUCOL- gates the RAM column address from the LA1+, 5+, 6+, 10+, C+, D+, E+, and F+ address lines to the RA0+-RA7+ bus through buffer 15B to the display RAMs. While the column address is valid on the RA0+-RA7+ lines from states 20 to 30, a single CAS- strobe occurs at state 26. Corresponding to the refresh cycle described above, LDP+ goes high at state 22 and LOAD1+ goes high at state 26 to move the RAM data to the video shift-registers.

If a display memory write cycle is being performed, WR- and DISPEN- (Display Enable) are low at pins 13 and 12 of gate 11B, respectively,

to generate WE- (Write Enable) at states 17 through 30. Write data is 16 bits, which is valid on the local data bus, LD0+-LDF+.

Memory Arbitration Logic

Display memory cycle requests can occur asynchronously with respect to the display memory controller state. The memory arbitration logic synchronizes these requests with the display memory controller by determining the start of the display memory cycle.

In case of a request during a nonrefresh (memory access) cycle, a display memory start signal occurs at pin 6 of gate 5E under the following conditions:

- o the local CPU is not ready at pin 1 of 5E,
- o the Multibus (IWS) CPU is not ready at pin 2 of 5E,
- o a display cycle is not occuring at pin 4 of 5E, and
- o a refresh cycle is not in progress at pin 5 of 5E.

When REFRESH+ goes high at pin 5 of 5E, pin 6 of 5E goes low. The low at pin 5 of RS flip-flop 6D causes pin 6 of 6D to go high, which arms the RS flip-flop. As soon as REFRESH- goes high at pin 1 of 6D, a low appears at pin 3 of 6D. The low is sent to the display memory RAM array as DISPEN- and is also inverted at pin 2 of 5D to start the memory controller state machine as DISPEN+. The DISPEN signals are active during the remainder of the display memory cycle and are cancelled when REFRESH- goes low at pin 1 of 6D, indicating that the memory controller is in a refresh cycle.

In a worst-case condition, a display memory cycle request can occur at the end of a refresh cycle. In this case, all of the inputs to gate 5E are high for only a short time and generate a pulse too short in duriation to set the RS flip-flop at 6D. The two 510-ohm resistors at R21 and R22, in conjunction with the 270-picofarad capacitor at C82, stretch the pulse from pin 6 of 5E to insure that 6D sets.

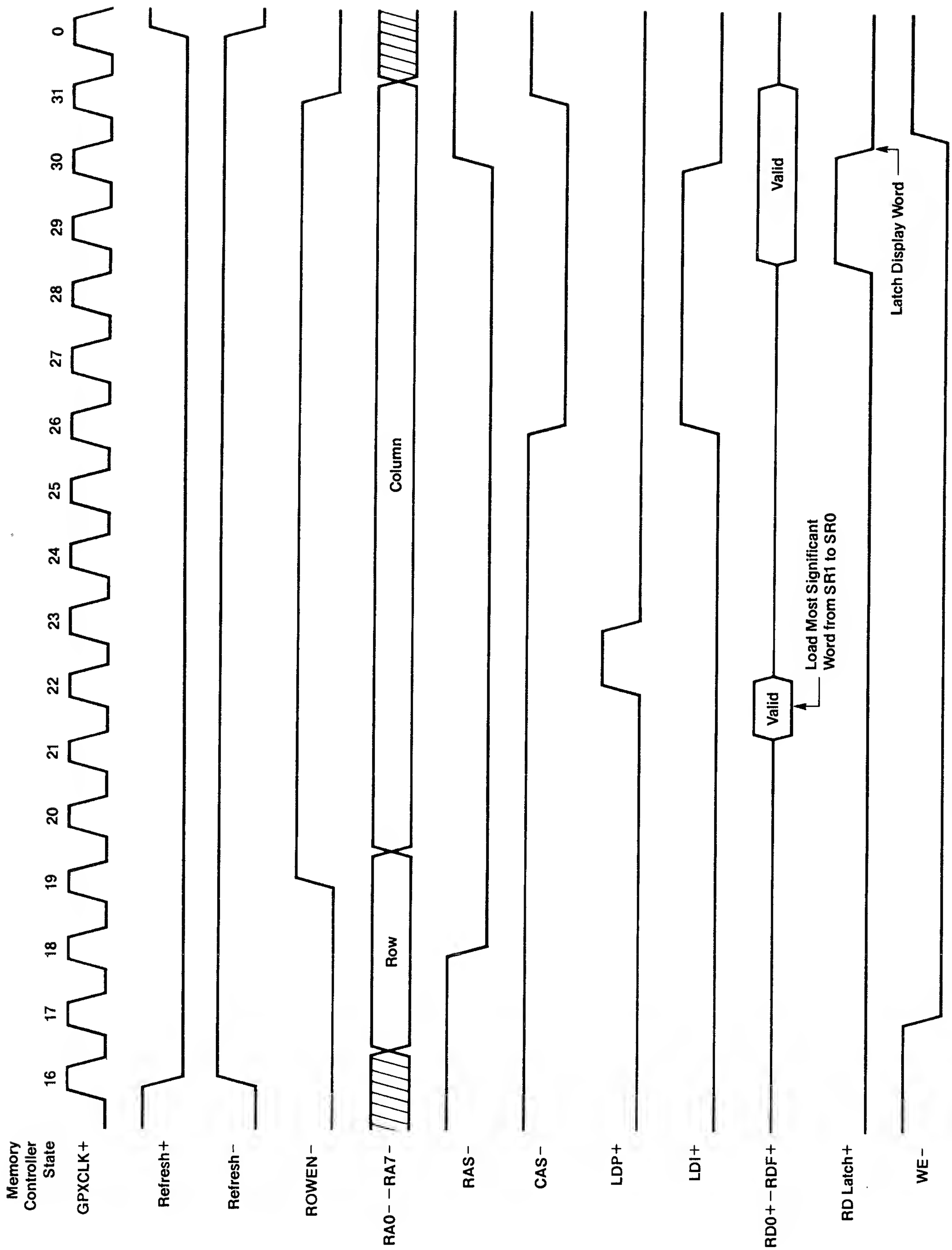


Figure 3-5. Display Memory Access Timing Diagram.

RAM Data Latches and Video Shift Registers

As shown on page 7 of Figure 3-2, data from the display memory appears on the RD0+-RDF+ (RAM Data) lines and can be sent either to the data bus latches during a read cycle, or the video shift-registers during a refresh cycle.

During a display memory read cycle, 16 bits of display memory data can be transferred to the local data bus via latches 17C and 20C when RDLATCH+ occurs at the end of the display memory access cycle. The outputs of 17C and 20C are enabled only during a valid memory read cycle by DISPCYC+ being NANDed at pin 13 of gate 12C with its qualifier, an inverted RD- strobe at pin 12. The resulting low at pin 11 of 12C enables the 16 bits of display memory data onto the local data bus lines, LD0+-LDF+.

The video shift-registers at 16C, 18C, 15C, and 19C are used to hold and then serialize two 16-bit words read from the display memory during a display memory refresh cycle. The shift registers are initially cleared by LOCBLANK- (Local Blank) from the bit 1 output of Control Register 12B (see page 5 of Figure 3-2). The words are then synchronized by the state machine described above, converted to ECL levels, and sent to the IWS Video Board.

As shown in the Memory Refresh Timing Diagram, Figure 3-4 above, LDP+ occurs at state 6 to load the least significant (first) word read from RAM on the RD0+-RDF+ (RAM Data Output) lines into SR0 (Shift Regsiter 0), the shift register pair 15C and 19C. LDP+ appears at the pin 19 S1 mode inputs of the SR0 shift registers to cause (along with the high at the pin 1 S0 mode inputs) a parallel loading of the data bits at the shift register inputs A through H. At state 7, the positive transition of GPXCLK+ at pin 12 of 15C and 19C, loads the most significant word into SR0.

Once SR0 is loaded, LDP+ goes low, changing SR0's mode to allow serial shifting of the word bits from 19C's QH output as VIDEO+. For each positive transition of GPXCLK+, 15C shifts a bit of the word from its QH output to the SR input of 19C at pin 11. Simultaneously, bits are shifted out of 19C's QH output as VIDEO+ to the state

machine for synchronization. (See page 4 of Figure 3-2.)

By state 14 of the cycle, SR0 has shifted out eight bits of the word. LOAD1+ (Load Shift Register 1) goes high to the S0 and S1 inputs of SR1 at shift registers 16C and 18C, which causes them to load the most significant (second) word of the display memory refresh cycle at the next transition of GPXCLK+. SR0 continues to shift out bits from the first word until state 22 (see Figure 3-5 above) when it is ready to shift out the last of the 16 bits. The combination of a low LDP- (the complement of LDP+ used to load SR0) and REFRESH+ causes SR1 to place the word previously stored, back onto the RD0+-RDF+ lines. Simultaneously, LDP+ goes high to the S1 inputs of SR0, causing the word from SR1 to be latched into SR0, as before, on the next positive transition of GPXCLK+. LDP+ then goes low again and the bits are shifted out of 19C's QH output as VIDEO+.

The VIDEO+ bits from pin 17 of 19C are sent to the pin 4 input of 9B (see page 4 of Figure 3-2) to be synchronized to GPXCLK+. The clocked bits are then sent back to pin 12 of a resistor network at 2A (see page 7 of Figure 3-2) as VIDEOS+ (Synchronized Video). VIDEOS+ is converted to an ECL level at 2A and sent to the pin 10 input of ECL NAND gate 6B. If VIDEOS+ is not blanked at pin 11 of 6B, it is gated to the IWS Video Board as EVIDEO+ (ECL Video) from pin 14 of 6B.

Blanking Logic

During periods of horizontal or vertical beam retrace, blanking circuitry is used to disallow video data from appearing on the display. EHORBLKS+ and VERTBLK+, from the Video Board, signal the blanking flip-flop 13C to blank the graphics video output, EVIDEO+. When a horizontal blank occurs, BEGHBLK- (discussed above under "Display Memroy Cycle Generation and Timing") sets 13C's pin 6 output to a low as BLANK-. BLANK- disables pin 11 of 6B, which disables the EVIDEO+ bit stream to the Video Board. When the horizontal blank period ends, HORBLK- goes high to clock pin 3 of 13C. If VERTBLK+ is high at pin 2 of 13C, the vertical retrace is beginning and a low is clocked through

to pin 6 of 13C continuing the blanking signal. If VERTBLK+ is low, the vertical retrace is complete and a high is clocked to pin 6 of 13C. A high then appears at pin 11 of 6B, allowing EVIDEO+ to sent graphics video to the Video Board for another horizontal scan line of the display.

CPU Ready Logic

Because the display RAM requires a greater access time than the static RAM or EPROM, the 8086-2 at 22D requires a ready signal to begin a display memory cycle. The ready signal, CPURDY+ (see page 4 of Figure 3-2) comes from flip-flop 13C. When ALE- goes high, that is, ALE+ from the 8086-2 has latched an address, 13C clocks the state of DISPLAYS- (Display Cycle Select) to the Q output at pin 9 as CPURDY+. If DISPLAYS- is low, meaning that the 8086-2 address has decoded a display memory cycle, CPURDY+ goes low to disable a subsequent display memory cycle.

CPURDY+ is also disabled when the IWS CPU is accessing the display memory to prevent the 8086-2 from attempting a cycle. SLAVE- (from the Multibus interface logic), resets pin 13 of 13C when a Multibus access it taking place.

CPURDY+ is set at the end of the display memory cycle by the NAND of RDLATCH+ and a high SLAVE- at pins 1 and 2 of gate 4E. The resulting low at pin 3 of 4E sets flip-flop 13C, thus causing CPURDY+ go high at pin 9 to the RDY1 input of 8284A 22C (see page 2 of Figure 3-2). The 8284A synchronizes CPURDY+ with the processor clock and sends the ready signal to the 8086-2 as RDY+.

APPENDIX G: UPDATED IWS SCHEMATICS

IWS Motherboard Wirelist

SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH: A	COMM CH: B	DISK	KYBD. J	KYBD. J	PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	10	17	J11	J12	J13	J14	J15	J16	MB1	MB2
BCLK-			9															13	13
INIT-			10															14	14
BPRNØ-			11																
BPRN1-																		15	
BPRN2-																			15
BUSY-			13															17	17
BREQØ-			14																
BREQ1-																		18	
BREQ2-																			18
MRDC-			16															19	19
MWTC-			17															20	20
IORC-			18															21	21
IOWC-			19															22	22
XACK-			20															23	23
INH1-			21															24	24
RESERVED			22								2							25	25
INH2-			23															26	26
BHEN-			24															27	27
ADIO-			26															28	28
ADI1-			28															30	30
ADI2-			30															32	32
ADI3-			32															34	34
CBRQ-			27															29	29
CCLK-			29															31	31
INTA-			31															33	33
INT7B-			33		34				*									36	36
INT6-			34															35	35
INT5-			36															38	38

SIGNAL	MEM EXP J1	CPU J2	CPU J3	I/O-MEM J4	I/O-MEM J5	VIDEO J6	COMM CH. A J7	COMM CH. B J8	DISK J9	KYBD. J10	KYBD. J17	PRINTER J11	PWR. J12	VIDEO J13	MONITOR J14	DAISY CHAIN J15	DAISY CHAIN J16	MB1	MB2
INT4B-			37		37				*									37	37
INT3-			▷38		87◁													40	40
INT2-			39															39	39
INT1B-			40		40				*									42	42
INTØ-			41															41	41
SIOACK-			42		42														
SIORQ+			43		43														
RDHIPEA-			44		44														
LBHEN+			46																
RDLOPEA-			47		47														
MW-			48		48														
DISKACK-			49		49														
DISKRQ+			50		50														
ODDP+			51		51														
WAIT-			52			44													
IOBCS+			53		53														
IOR-			54		54	46													
DCIRDY+			56		56														
FASTIO+			57		57														
DMACTCS-			58		58														
DMACS-			59		59														
IOB7+			60		60														
IOB6+			61		61														
IOB5+			62		62														
IOB4+			63		63														
IOB3+			64		64														
IOB2+			66		66														
IOB1+			67		67														

SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH: B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J17	J11	J12	J13	J14	J15	J16	MB1	MB2
IOBØ+			68		68														
DREQ-					69				35										
IOCS-			70		70														
NMI+			71		71														
PICCS-			72		72														
MEMCLK+			73		73	9													
TEST			74								3								
LPTACK-					74							16							
IOW-			76		76	14													
EOP-			77		77	11													
VIDACK-			78			17													
PERINT-			79		79														
MWINH-			80		80														
TCLK-					9		18									6 ▷	6 ▷		
TCLK+					10		25									7 ▷	7 ▷		
RXDA-					11		3												
CTSA+					12		5												
RXCA+					13		17									6 ▷	6 ▷		
TXCA+					14		15									7 ▷	7 ▷		
DSRA+					16		6												
SRDA+					17		16												
STDA-					18		14												
TXDA-					19		2									8 ▷	8 ▷		
RTSA+					20		4									9 ▷	9 ▷		
DTRA+					21		20												
DCDA+					22		8									8 ▷	8 ▷		
RINGA+					23		22									9 ▷	9 ▷		
CTSB+					24			5					(SEE	NOTE	▷	SHEET	16)		

SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH. B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J 10	J 17	J11	J12	J13	J14	J15	J16	MB1	MB2
RXDB-					26			3											
TXCB+					27			15											
RXCB+					28			17											
DSRB+					29			6											
SRDB-					30			16											
DCDB+					31			8											
RINGB+					32			22											
DTRB+					33			20											
RTSB+					36			4											
STDB-					38			14											
TXDB-					39			2											
KBD1-					41					1									
KBDØ-					46					3									
ENBL-					52				18										
ADRF-			86															44	44
ADRE-			87															43	43
ADRD-			88															46	46
ADRC-			89															45	45
ADRB-			90															48	48
ADRA-			91															47	47
ADR9-			92															50	50
ADR8-			93															49	49
ADR7-			94															52	52
ADR6-			96															51	51
ADR5-			97															54	54
ADR4-			98															53	53
ADR3-			99															56	56
ADR2-			100															55	55

SIGNAL	MEM EXP J1	CPU J2	CPU J3	I/O-MEM J4	I/O-MEM J5	VIDEO J6	COMM CH. A J7	COMM CH. B J8	DISK J9	KYBD. J 16	KYBD. J 17	PRINTER J11	PWR. J12	VIDEO J13	MONITOR J14	DAISY CHAIN J15	DAISY CHAIN J16	MB1	MB2
ADR1-			101															58	58
ADRØ-			102															57	57
TØ+			81		81														
MBIO-			82		82														
RESET-			83		83	13													
PAREN-			84		84														
DATF-			103															60	60
DATE-			104															59	59
DATD-			106															62	62
DATC-			107															61	61
DATB-			108															64	64
DATA-			109															63	63
DAT9-			110															66	66
DAT8-			111															65	65
DAT7-			112															68	68
DAT6-			113															67	67
DAT5-			114															70	70
DAT4-			116															69	69
DAT3-			117															72	72
DAT2-			118															71	71
DAT1-			119															74	74
DATØ-			120															73	73
ACK-					86				2										
CNTRL-					88				20										
SELF-					89				4										
SELW-					90				37										
WRSTB-					91				22										
INRQ-					92				6										

SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH. B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J17	J11	J12	J13	J14	J15	J16	MB1	MB2
RDSTB-					93				39										
BUSØ+					94				24										
BUS1+					99				10										
BUS2+					96				8										
BUS3+					100				43										
BUS4+					97				41										
BUS5+					101				28										
BUS6+					98				26										
BUS7+					102				12										
BUS8+					107				47										
BUS9+					111				33										
BUSA+					106				14										
BUSB+					110				49										
BUSC+					104				30										
BUSD+					109				16										
BUSE+					103				45										
BUSF+					108				32										
LPTØ+					117							1							
LPT1+					112							2							
LPT2+					118							3							
LPT3+					113							4							
LPT4+					120							5							
LPT5+					114							6							
LPT6+					119							7							
LPT7+					116							8							
MR-	10	1		1		10													
VIDRQ+		2				16													
NO PAPER+				2								21							

SIGNAL	MEM EXP J1	CPU J2	CPU J3	I/O-MEM J4	I/O-MEM J5	VIDEO J6	COMM CH. A J7	COMM CH. B J8	DISK J9	KYBD. J10	KYBD. J17	PRINTER J11	PWR. J12	VIDEO J13	MONITOR J14	DAISY CHAIN J15	DAISY CHAIN J16	MB1	MB2
BD2RAM-	9	3																	
LPTBUSY+				3								17							
BD1RAM-		4		4															
COLMPX-	12	6		6															
RARAS-	14	7		7															
PROMEXDC-	11	8																	
BEOP-				8					48										
RFGO-	16	9		9															
RFDONE-	13	10		10															
RAHIWE-	18	11		11															
RALOWE-	17	12		12															
GACCS-				18		12													
78KHZ+		13		13															
SFØ				14									16						
CAS7-	19	14																	
CAS6-	20	16																	
CAS5-	21	17																	
CAS4-	22	18																	
CAS3-		19		19															
CAS2-		20		20															
CAS1-		21		21															
CASØ-		22		22															
LPT SELECT+				16								22							
AUDIO+				17															
HIP+	23	23		23															
LOP+	24	24		24															
MEMF+	26	26		26		26													
MEME+	27	27		27		27													

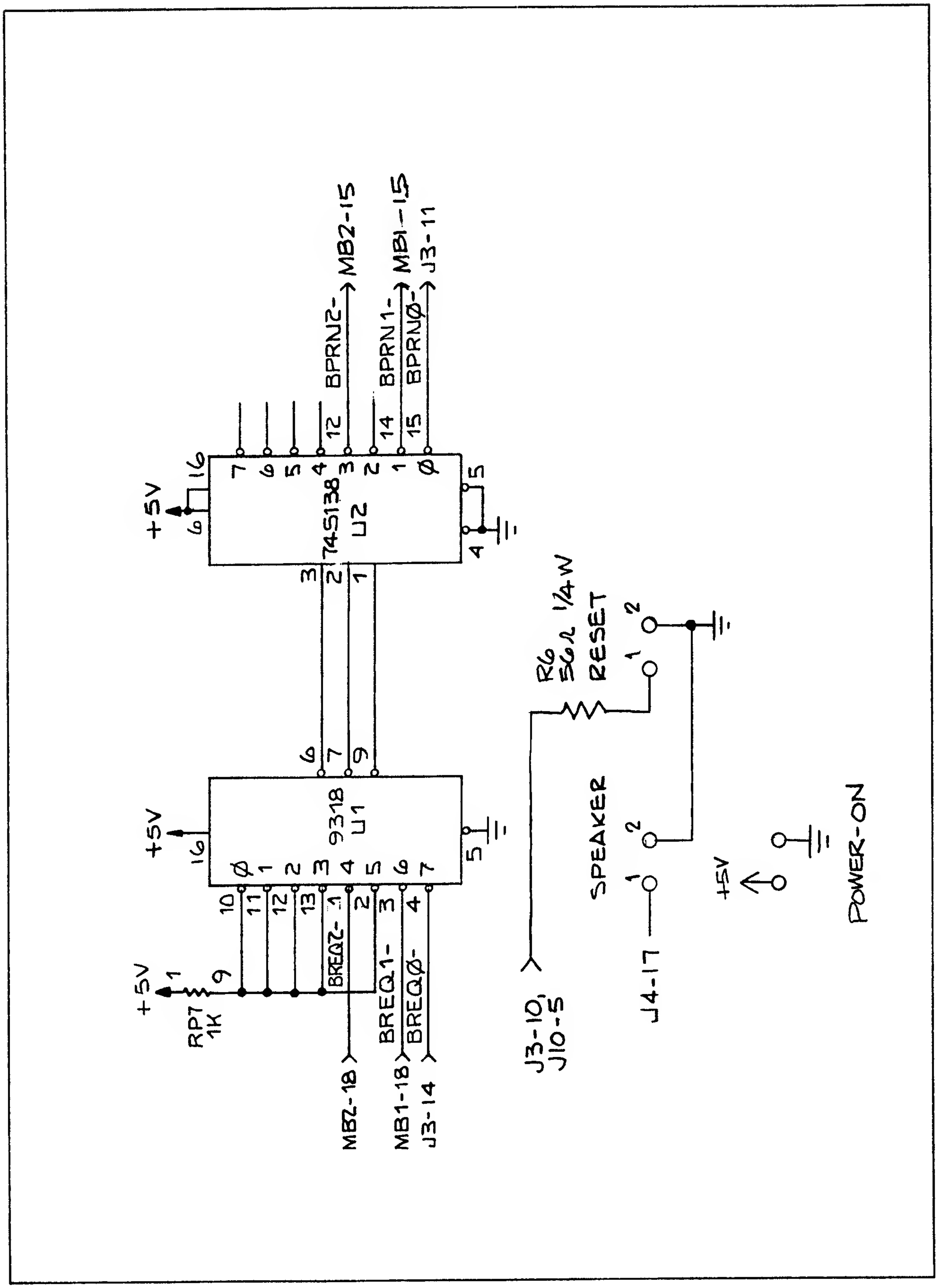
SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH: A	COMM CH: B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J 10	J 17	J11	J12	J13	J14	J15	J16	MB1	MB2
MEMD+	28	28		28		28													
MEMC+	29	29		29		29													
MEMB+	30	30		30		30													
MEMA+	31	31		31		31													
MEM9+	32	32		32		32													
MEM8+	33	33		33		33													
MEM7+	34	34		34		34													
MEM6+	36	36		36		36													
MEM5+	37	37		37		37													
MEM4+	38	38		38		38													
MEM3+	39	39		39		39													
MEM2+	40	40		40		40													
MEM1+	41	41		41		41													
MEMØ+	42	42		42		42													
LA13+	43	43		43															
LA12+	44	44		44															
LA11+	46	46		46															
LA10+	47	47		47															
LAF+	48	48		48		48													
LAE+	49	49		49		49													
LAD+	50	50		50		50													
LAC+	51	51		51		51													
LAB+	52	52		52		52													
LAA+	53	53		53		53													
LA9+	54	54		54		54													
LA8+	56	56		56		56													
LA7+	57	57		57		57													
LA6+	58	58		58		58													

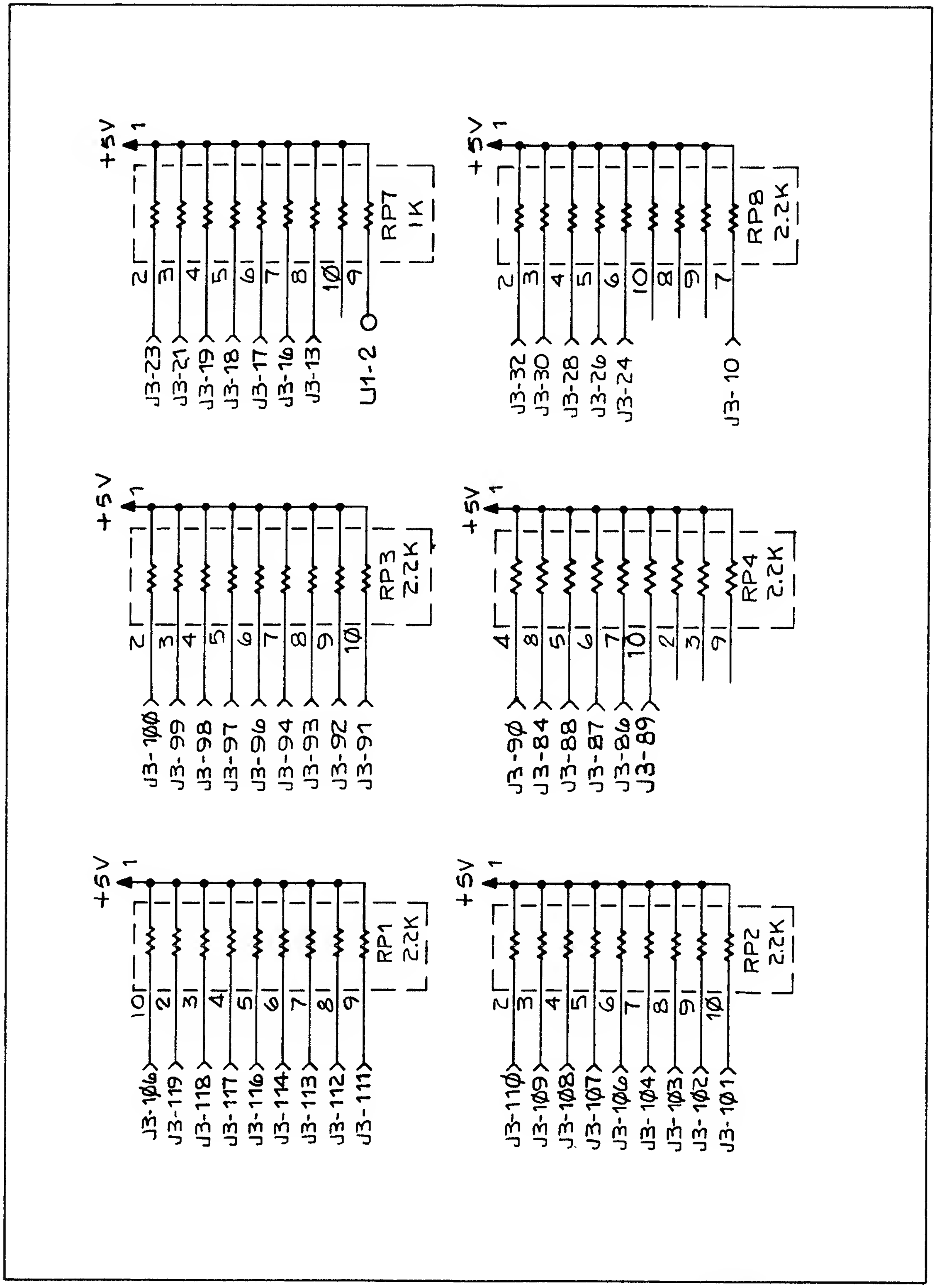
SIGNAL	MEM EXP J1	CPU J2	CPU J3	I/O-MEM J4	I/O-MEM J5	VIDEO J6	COMM CH. A J7	COMM CH. B J8	DISK J9	KYBD. J10	KYBD. J17	PRINT-ER J11	PWR. J12	VIDEO J13	MONI-TOR J14	DAISY CHAIN J15	DAISY CHAIN J16	MB1	MB2
LA5+	59	59		59		59													
LA4+	60	60		60		60													
LA3+	61	61		61		61													
LA2+	62	62		62		62													
LA1+	63	63		63		63													
LAØ+	64	64		64		64													
COMMTIMING		75		75															
		76									6								
STROBE-					78							14							
VIDEO A														1	10				
VIDEO A														3	9				
AUX VID B														7					
AUX VID A														8					
VIDEO B														4	12				
VIDEO B														6	13				
HOR DR														11	5				
HOR DR														13	4				
VERT DR														12	16				
VERT DR														14	17				
CRTOR														16	18				
BMR-				76					50										

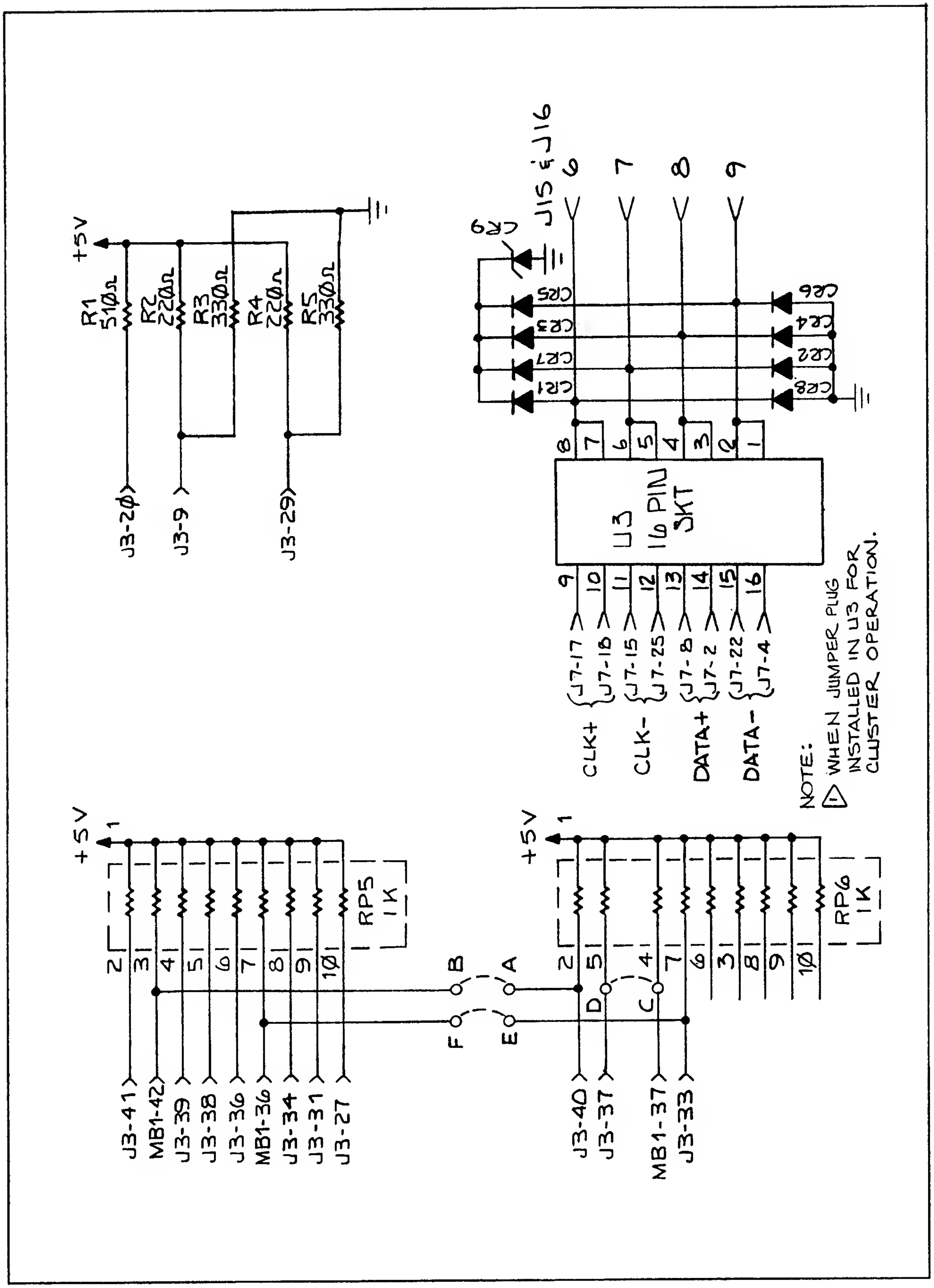
SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH: B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J17	J11	J12	J13	J14	J15	J16	MB1	MB2
+ 5V	1		1		1	1				6			1					3	3
	2		2		2	2				7			2					4	4
	3		3		3	3							3					5	5
	4		4		4	4							7					6	6
	77	77		77		77							10					81	81
	78	78		78		78							18					82	82
	79	79		79		79												83	83
+ 5V	80	80		80		80												84	84
+12V	67	67		67		67					1		5		20			7	7
	68	68		68		68							6					8	8
	69	69		69		69													
+ 12V	70	70		70		70													
−12V	5		5		5	5					4		8					79	79
	6		6		6	6												80	80
	73			73															
− 12V	74			74															
+32V													12		2				
−32V													14		1				

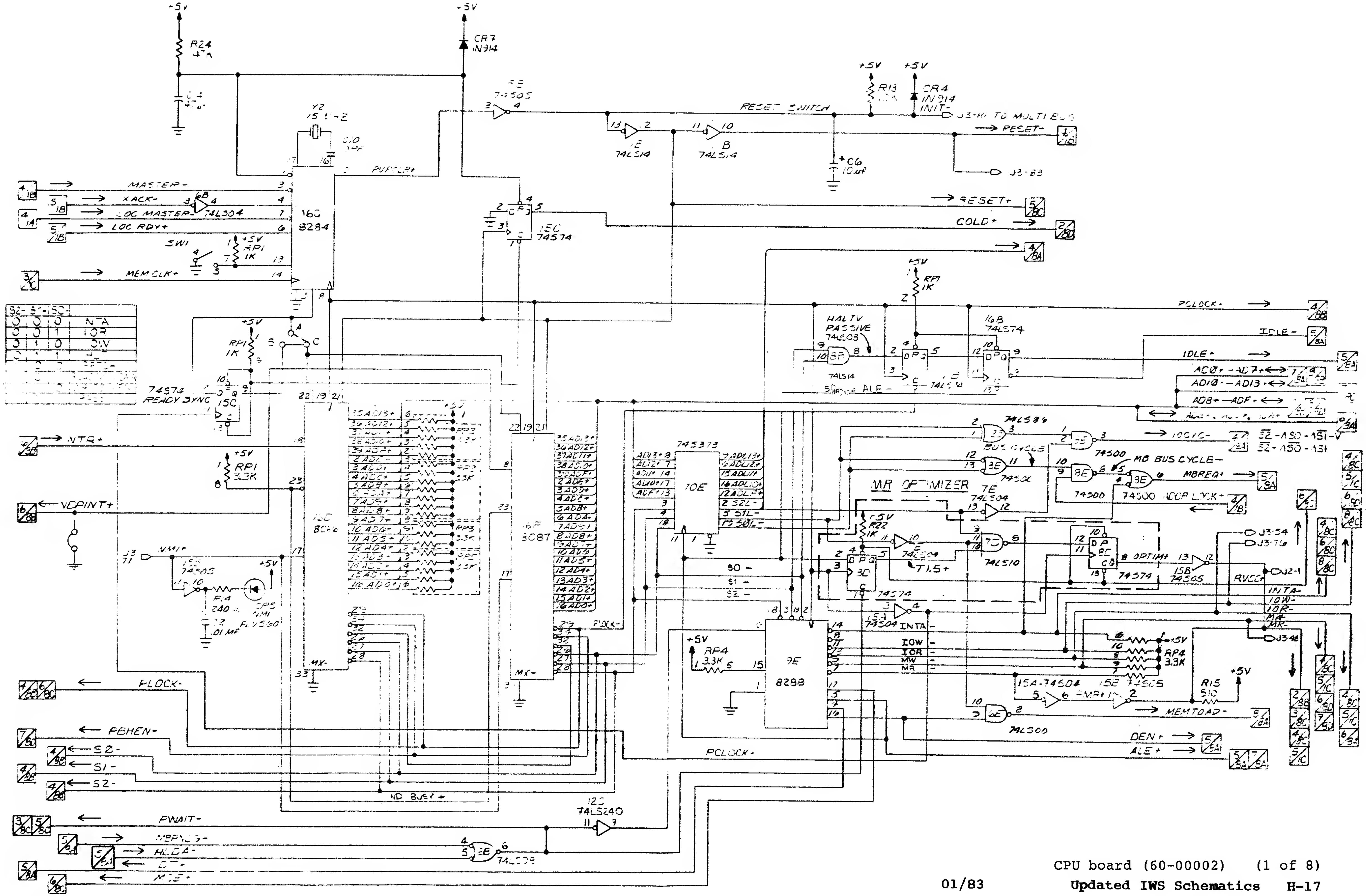
SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH: B	DISK	KYBD.		PRINT-ER	PWR.	VIDEO	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J 10	J 17	J11	J12	J13	J14	J15	J16	MB1	MB2
GND	7	5	7	5	7	7	1	1	1	2		9	4	2	11	1	1	1	1
	8		8		8	8	7	7	3	4		10	9	5	8	2	2	2	2
	15	15	15	15	15	15			5	9		11	11	9	6	3	3	11	11
	25	25	25	25	25	25			7	8		12	13	10	15	4	4	12	12
	35	35	35	35	35	35			9			15	15	15	3	5	5	75	75
						43			11			25	17	17				76	76
	45	45	45	45	45	45			13					18	19			85	85
						47			15					19				86	86
	55	55	55	55	55	55			17					20					
	65	65	65	65	65	65			19										
	66	66		66		66			21										
	71	71		71		71			23										
	72	72		72		72			25										
			75		75				27										
			85		85				29										
			95		95				31										
			105		105				34										
			115		115				36										
						18			38										
						21			40										
						24			42										
									44										
GND									46										

SIGNAL	MEM EXP	CPU	CPU	I/O-MEM	I/O-MEM	VIDEO	COMM CH. A	COMM CH. B	DISK	KYBD.		PRINT-ER	PWR.	VIDED	MONI-TOR	DAISY CHAIN	DAISY CHAIN		
	J1	J2	J3	J4	J5	J6	J7	J8	J9	J 10	J 17	J11	J12	J13	J14	J15	J16	MB1	MB2
SPARE							9	9		5	5	13			7			9	9
							10	10		10		18			14			10	10
							11	11				19						77	16
							12	12				20						78	77
							13	13				23							78
							19	18				24							
							21	19											
							23	21											
							24	23											
								24											
SPARE								25											

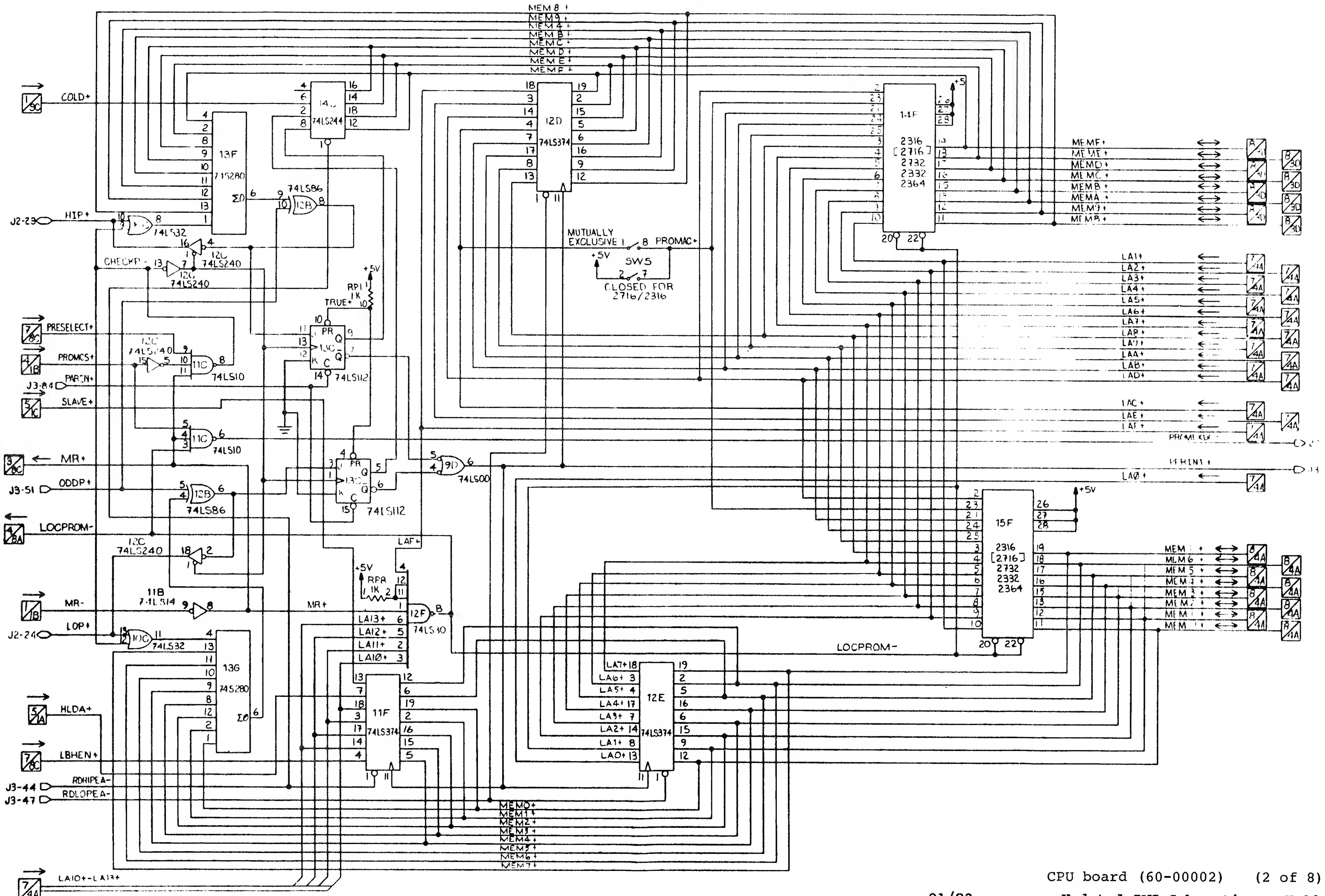

+5V
RP7
1K
BREQ2-
BREQ1-
BREQØ-
MB2-18
MB1-18
J3-14
9318
U1
74S138
U2
BPRN2-
BPRN1-
BPRNØ-
MB2-15
MB1-15
J3-11
R6
56Ω 1/4W
RESET
SPEAKER
POWER-ON
J3-10,
J10-5
J4-17


+5V
RP7
1K
J3-23
J3-21
J3-19
J3-18
J3-17
J3-16
J3-13
U1-2
RP8
2.2K
J3-32
J3-30
J3-28
J3-26
J3-24
J3-10
RP3
2.2K
J3-100
J3-99
J3-98
J3-97
J3-96
J3-94
J3-93
J3-92
J3-91
RP4
2.2K
J3-90
J3-84
J3-88
J3-87
J3-86
J3-89
RP1
2.2K
J3-106
J3-119
J3-118
J3-117
J3-116
J3-114
J3-113
J3-112
J3-111
RP2
2.2K
J3-110
J3-109
J3-108
J3-107
J3-106
J3-104
J3-103
J3-102
J3-101

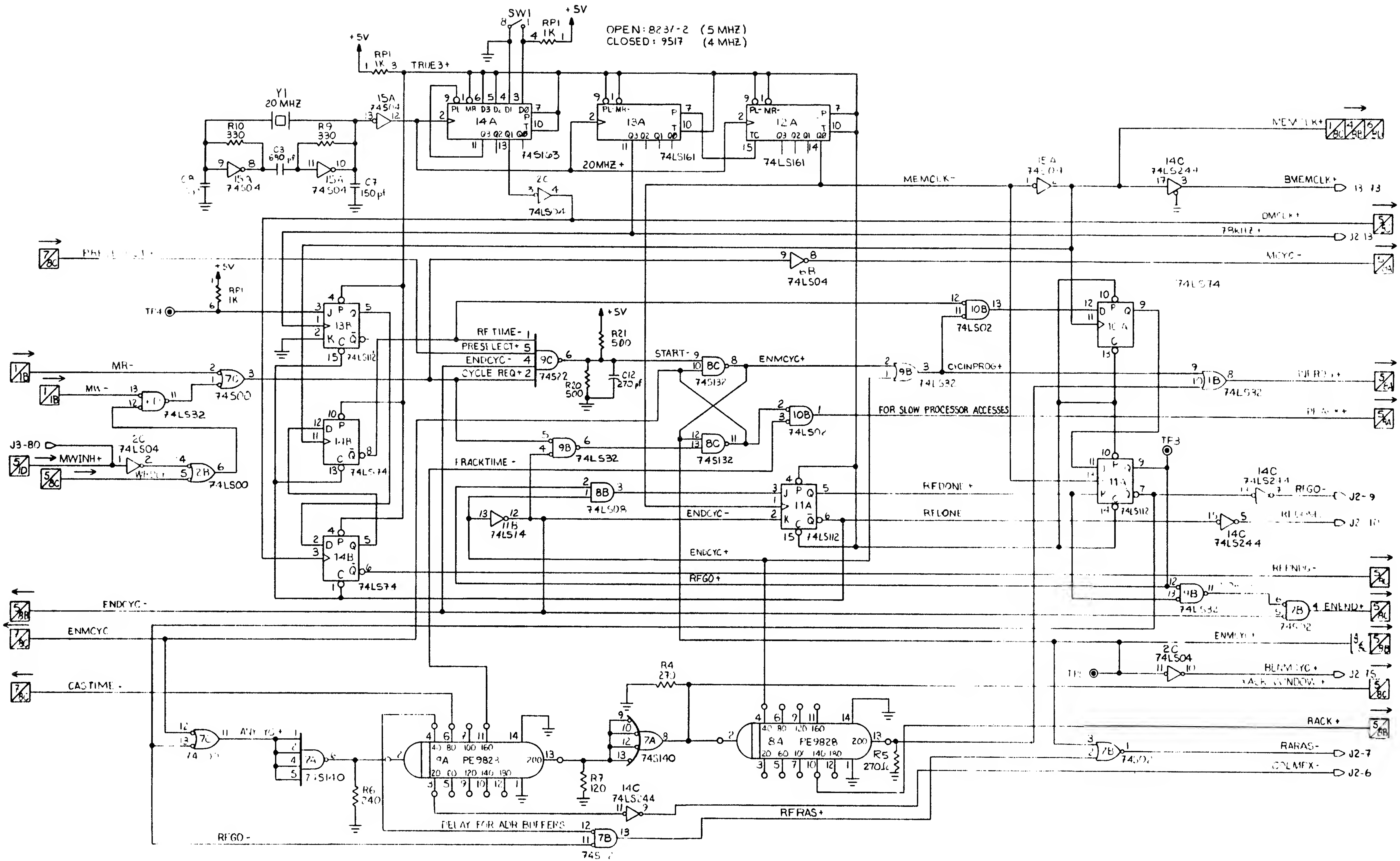

+5V
R1 51Ø Ω
R2 22Ø Ω
R3 33Ø Ω
R4 22Ø Ω
R5 33Ø Ω
J3-2Ø
J3-9
J3-29
J15 & J16
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
U3 16 PIN SKT
CLK+
CLK-
DATA+
DATA-
J7-17
J7-18
J7-15
J7-25
J7-8
J7-2
J7-22
J7-4
NOTE:
WHEN JUMPER PLUG INSTALLED IN U3 FOR CLUSTER OPERATION.
RP5 1K
RP6 1K
J3-41
MB1-42
J3-39
J3-38
J3-36
MB1-36
J3-34
J3-31
J3-27
J3-40
J3-37
MB1-37
J3-33

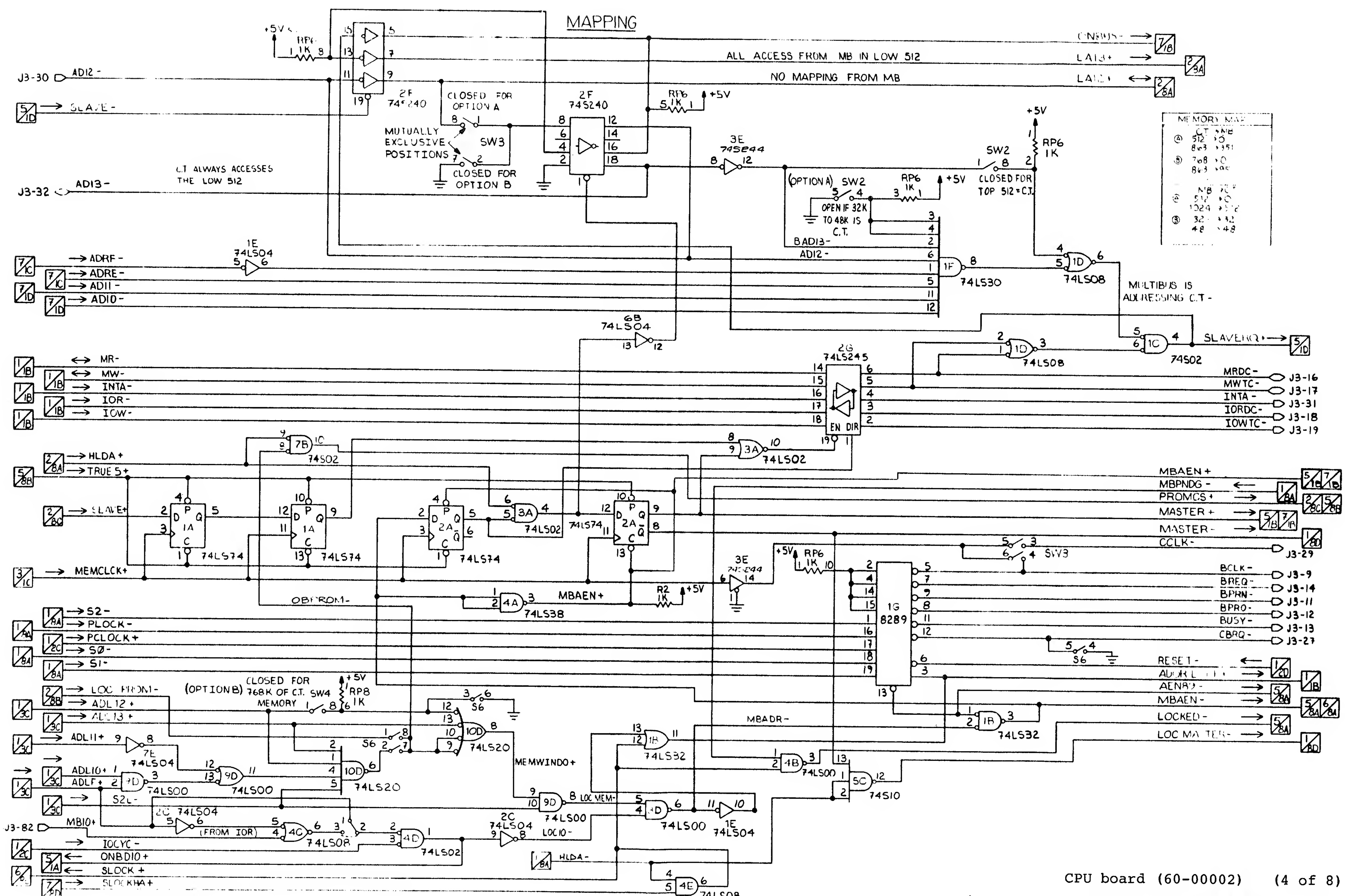


CPU board (60-00002) (1 of 8)

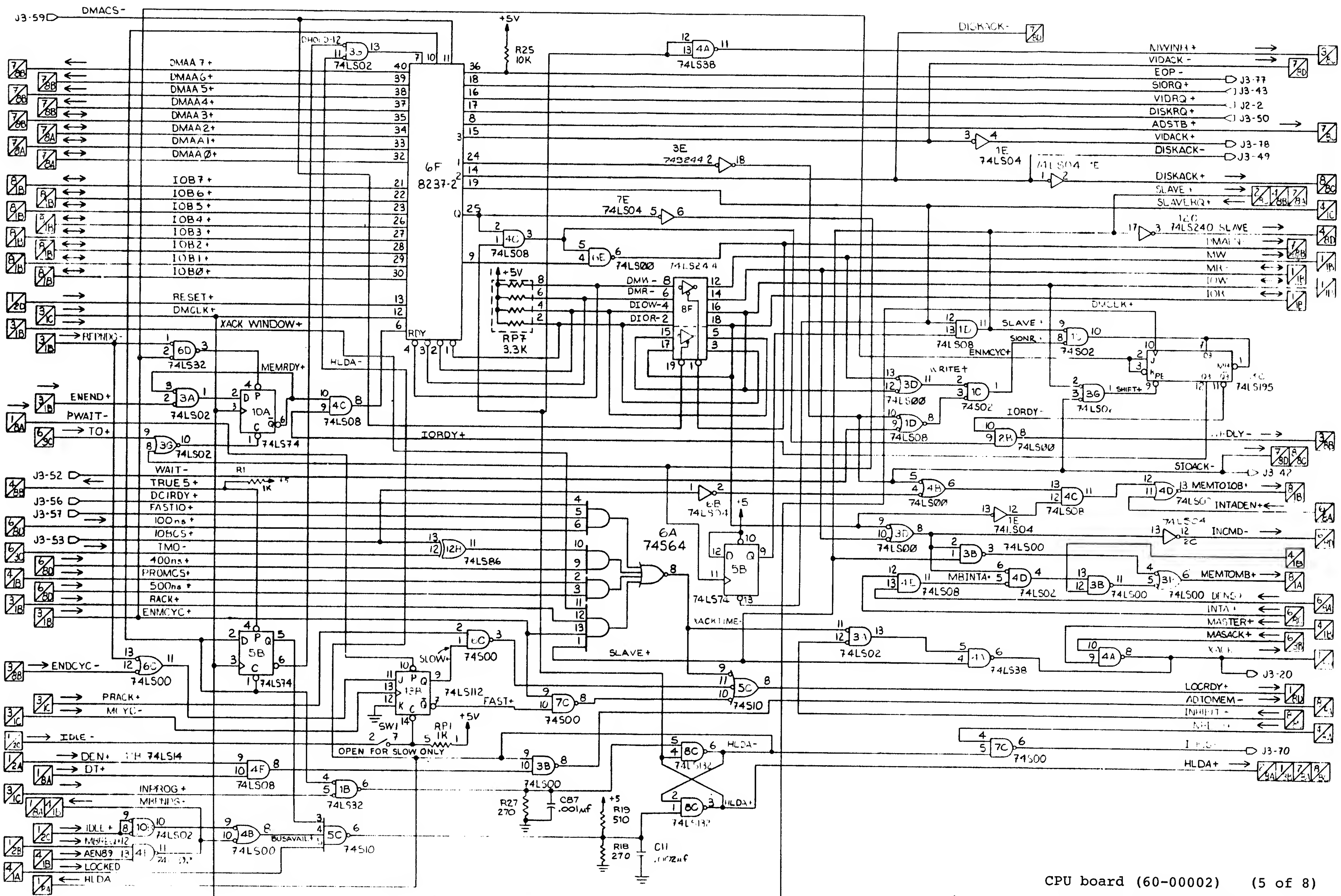


CPU board (60-00002) (2 of 8)

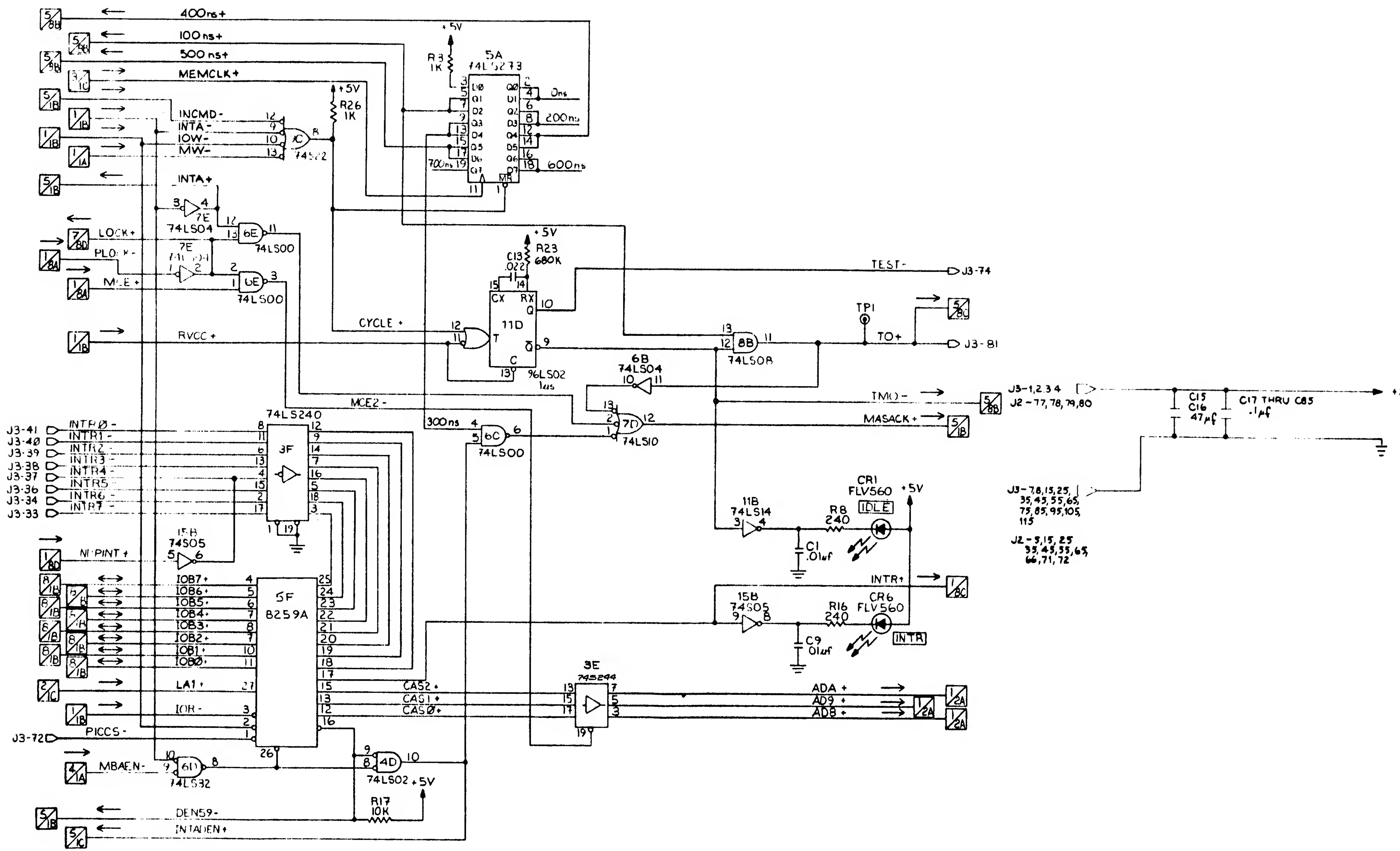

OPEN: 8237-2 (5 MHZ)
CLOSED: 9517 (4 MHZ)
SW1
RP1 1K
+5V
TRUE3+
Y1 20 MHZ
R10 330
R9 330
C3 680 pf
C7 150 pf
74S04
15A
14A
74S163
13A
74LS161
12A
20MHZ+
2C
74LS04
MEMCLK-
MEMCLK+
14C
74LS244
BMEMCLK+
DMCLK+
78KHZ+
MCYC-
6B
74LS74
TP4
13B
74LS112
MR-
MW-
7C
74S00
74LS32
J3-80
MWINH+
2B
74LS00
14B
RF TIME-
PRESELECT+
ENDCYC-
CYCLE REQ+
9C
74S22
R21 500
R20 500
C12 270 pf
START-
8C
74S132
ENMCYC+
9B
CYCINPROG+
10B
74LS02
FOR SLOW PROCESSOR ACCESSES
RFDONE+
RFLONE
11A
TP3
RFGO-
J2-9
J2-10
TRACKTIME-
8B
74LS08
11B
74LS14
ENDCYC+
RFGO+
RFEND-
ENEND+
7B
74S02
ENDCYC-
ENMCYC
ENMCYC+
BENMCYC+
J2-15
ACK WINDOW+
RACK+
RARAS-
J2-7
COLMPX-
J2-6
CASTIME-
R4 270
7A
74S140
9A
PE9828
8A
R5 270
R6 240
R7 120
RFRAS+
DELAY FOR ADR BUFFERS
RFGO-

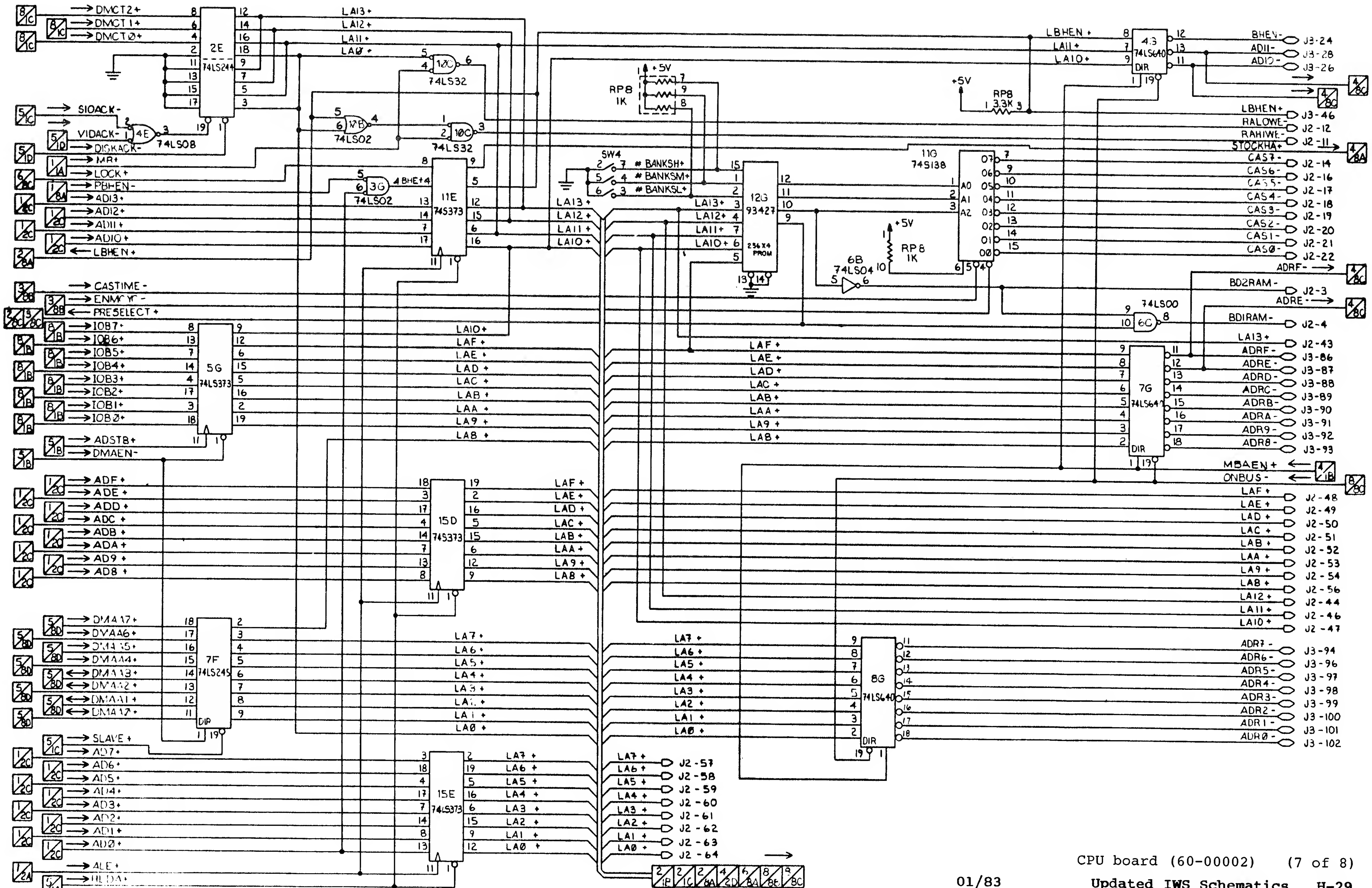


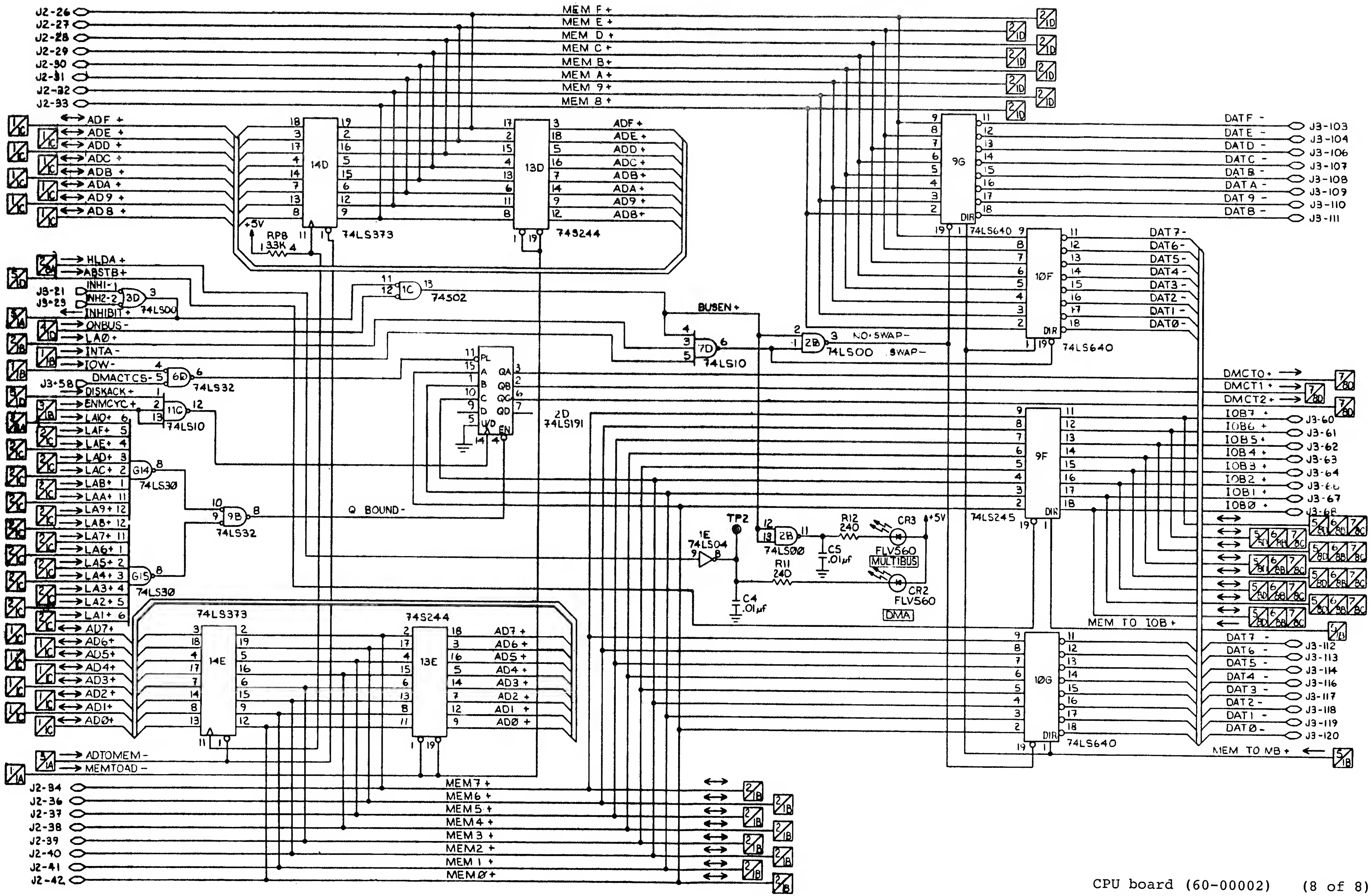
CPU board (60-00002) (4 of 8)



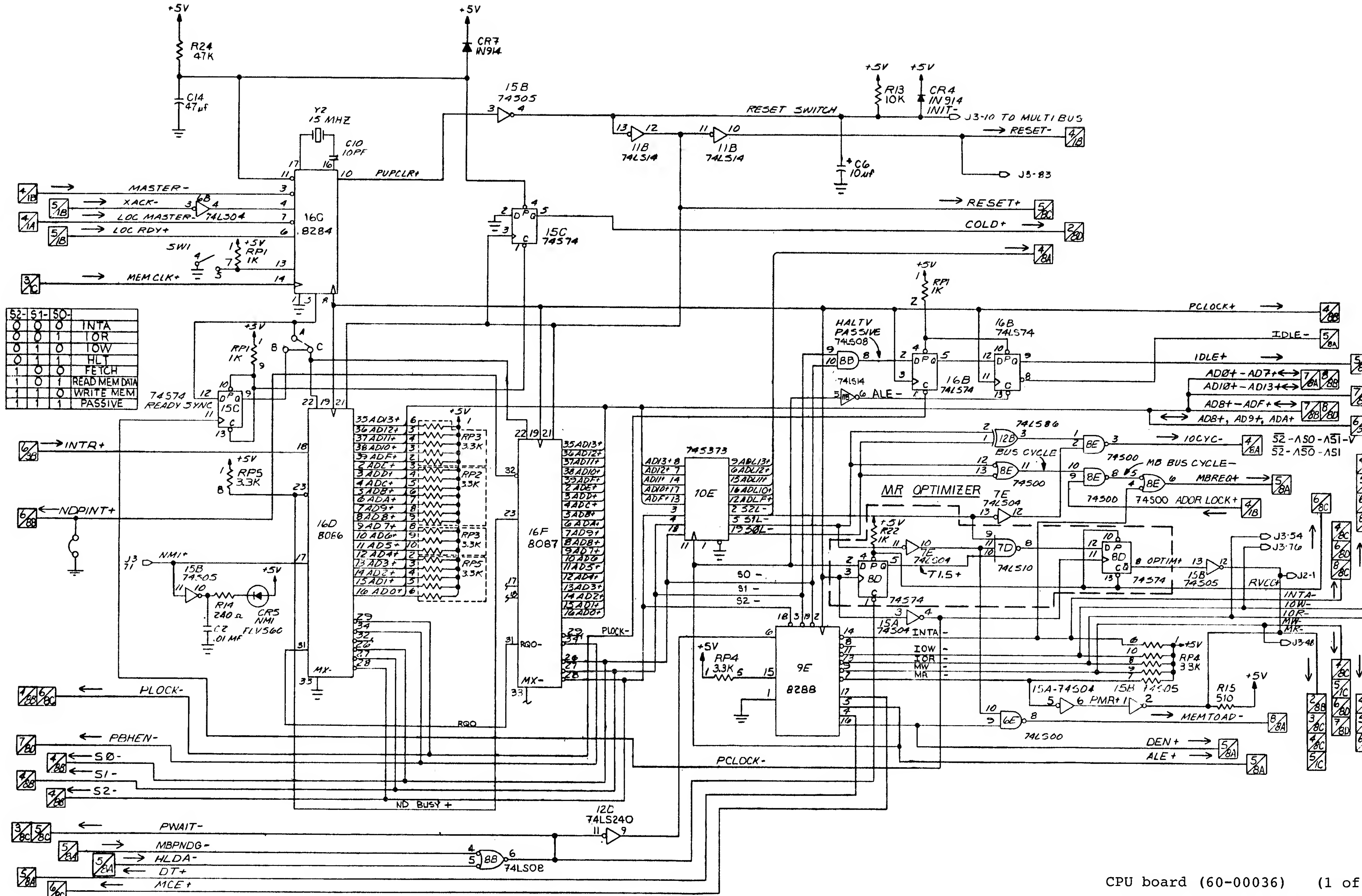
DMACS-
J3-59
+5V
R25
10K
6F
8237-2
74LS02
74LS38
74LS04
74LS08
74LS00
74LS244
8F
RP7
3.3K
74LS32
74LS74
10A
MEMRDY+
XACK WINDOW+
RESET+
DMCLK+
DMAA7+
DMAA6+
DMAA5+
DMAA4+
DMAA3+
DMAA2+
DMAA1+
DMAAØ+
IOB7+
IOB6+
IOB5+
IOB4+
IOB3+
IOB2+
IOB1+
IOBØ+
ENEND+
PWAIT-
TO+
WAIT-
TRUE5+
DCIRDY+
FASTIO+
100ns+
IOBCS+
TMO-
400ns+
PROMCS+
500ns+
RACK+
ENMCYC+
ENDCYC-
PRACK+
MCYC-
IDLE-
DEN+
DT+
INPROG+
MBENDS-
LOCKED
HLDA
HLDA-
HLDA+
IORDY+
IORDY-
6A
74S64
74LS86
74S00
74LS112
SLOW+
FAST+
SW1
OPEN FOR SLOW ONLY
RP1
1K
R27
270
C87
.001μf
R19
510
R18
270
C11
74S10
74LS195
SLAVE+
SIONR
ENMCYC+
WRITE+
SHIFT+
DIOW-4
DIOR-2
DMW-8
DMR-6
MWINH+
VIDACK-
EOP-
SIORQ+
VIDRQ+
DISKRQ+
ADSTB+
VIDACK+
DISKACK-
DISKACK+
SLAVE+
SLAVERQ+
74LS240 SLAVE
MW
MR
IOW
IOR
DMCLK+
STOACK-
MEMTOIOB+
INTADEN+
INCMD-
MBINTA+
MEMTOMB+
DENSO
INTA+
MASTER+
MASACK+
XACK
LOCRDY+
ADTOMEM-
INHIBIT+
XACKTIME-
BUSAVAIL+
J3-77
J3-43
J2-2
J3-50
J3-78
J3-49
J3-42
J3-20
J3-70
J3-52
J3-56
J3-57
J3-53





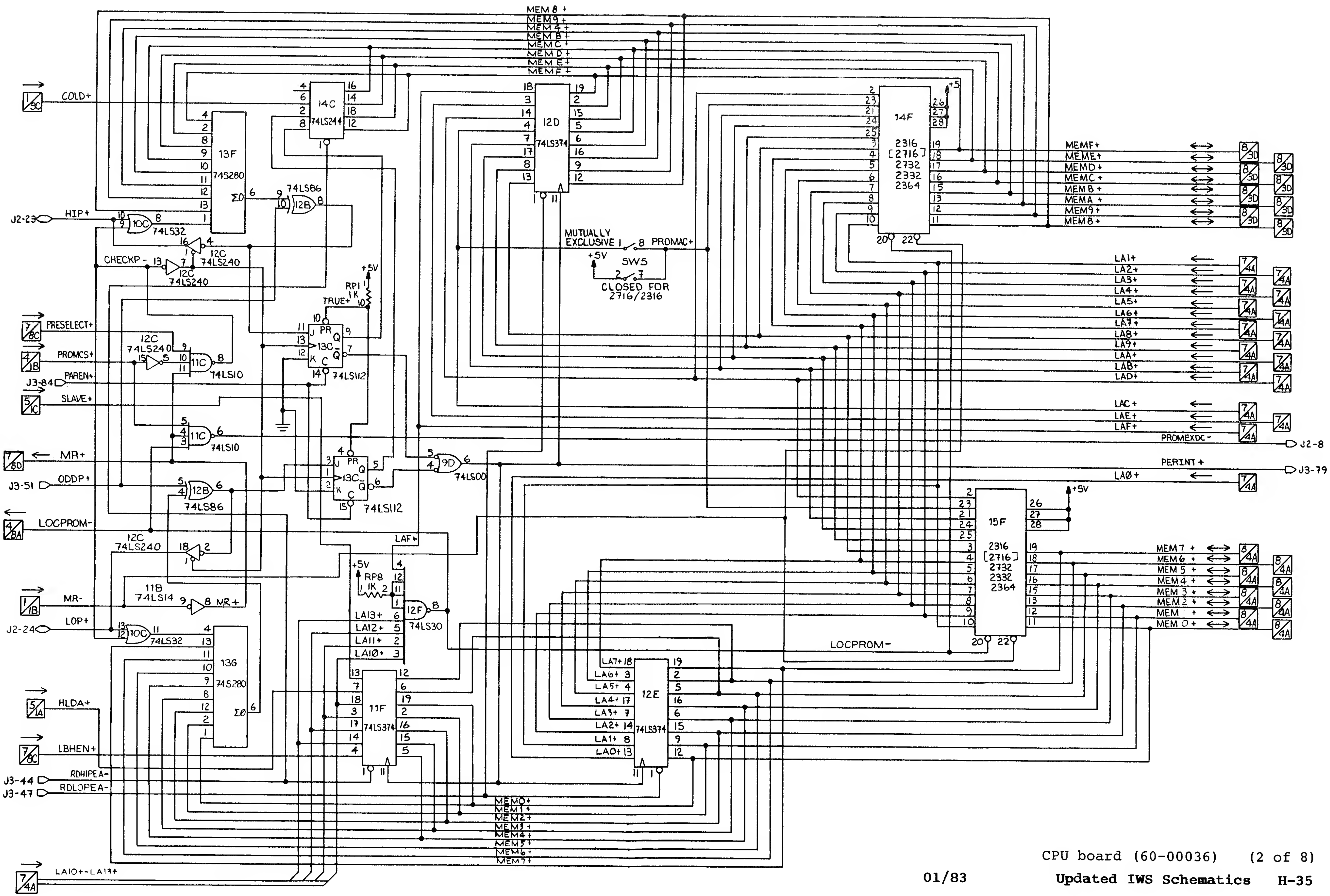


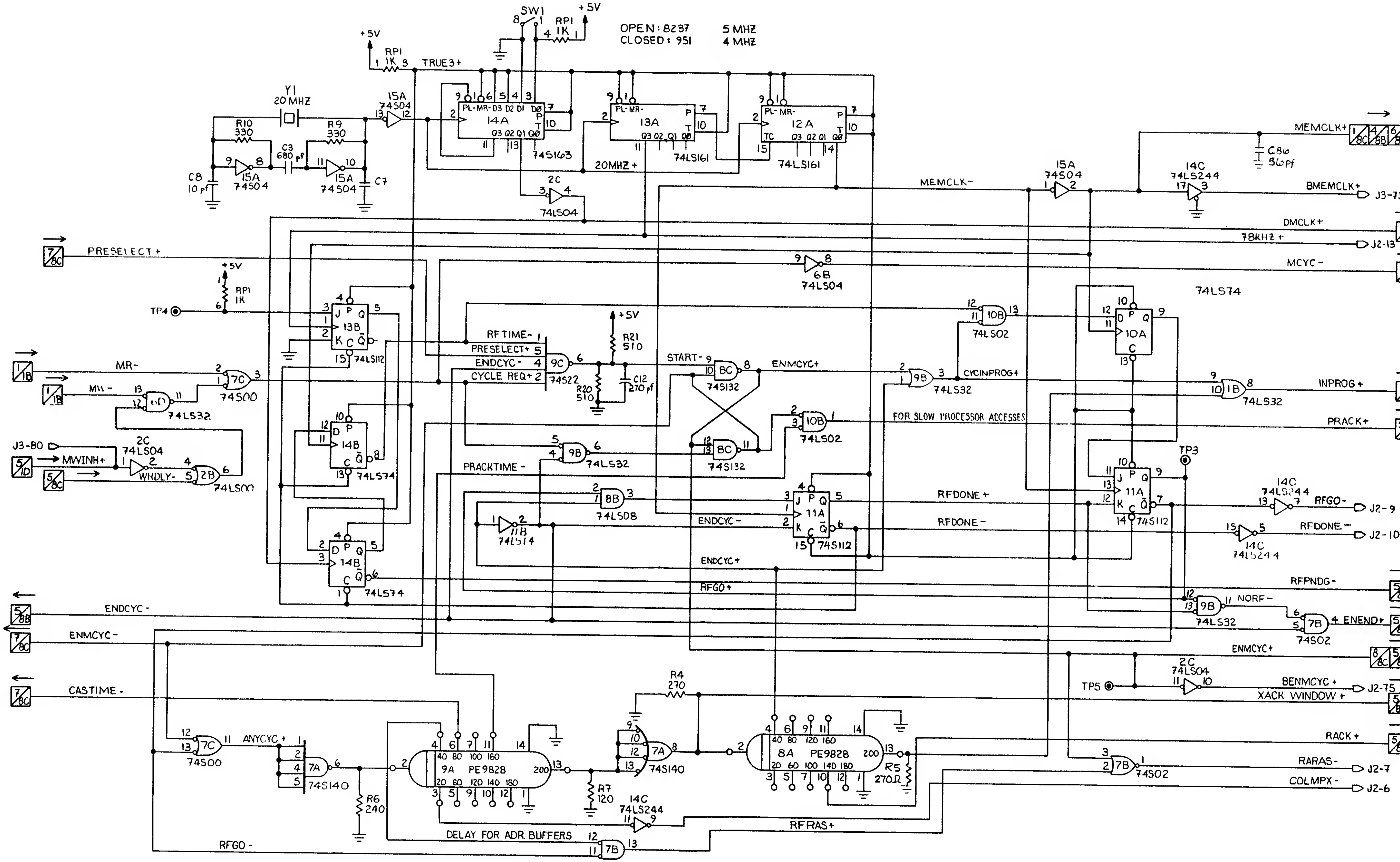
MEM F +
MEM E +
MEM D +
MEM C +
MEM B +
MEM A +
MEM 9 +
MEM 8 +
14D
13D
74LS373
74S244
9G
74LS640
10F
74LS640
DATF -
DATE -
DATD -
DATC -
DATB -
DATA -
DAT9 -
DAT8 -
DAT7-
DAT6-
DAT5-
DAT4-
DAT3-
DAT2-
DAT1-
DATØ-
HLDA +
ABSTB +
INHIBIT +
ONBUS -
LAØ +
INTA -
IOW -
DMACTCS -
DISKACK +
ENMCYC +
74LS00
74S02
BUSEN +
74LS10
NO-SWAP-
SWAP-
2D
74LS191
74LS32
74LS30
Q BOUND-
DMCT0 +
DMCT1 +
DMCT2 +
9F
74LS245
IOB7 +
IOB6 +
IOB5 +
IOB4 +
IOB3 +
IOB2 +
IOB1 +
IOBØ +
TP2
74LS04
R12 240
R11 240
C5 .01µf
C4 .01µf
CR3 FLV560
MULTIBUS
CR2 FLV560
DMA
MEM TO IOB +
10G
MEM TO MB +
14E
13E
ADTOMEM -
MEMTOAD -
MEM7 +
MEM6 +
MEM5 +
MEM4 +
MEM3 +
MEM2 +
MEM1 +
MEMØ +



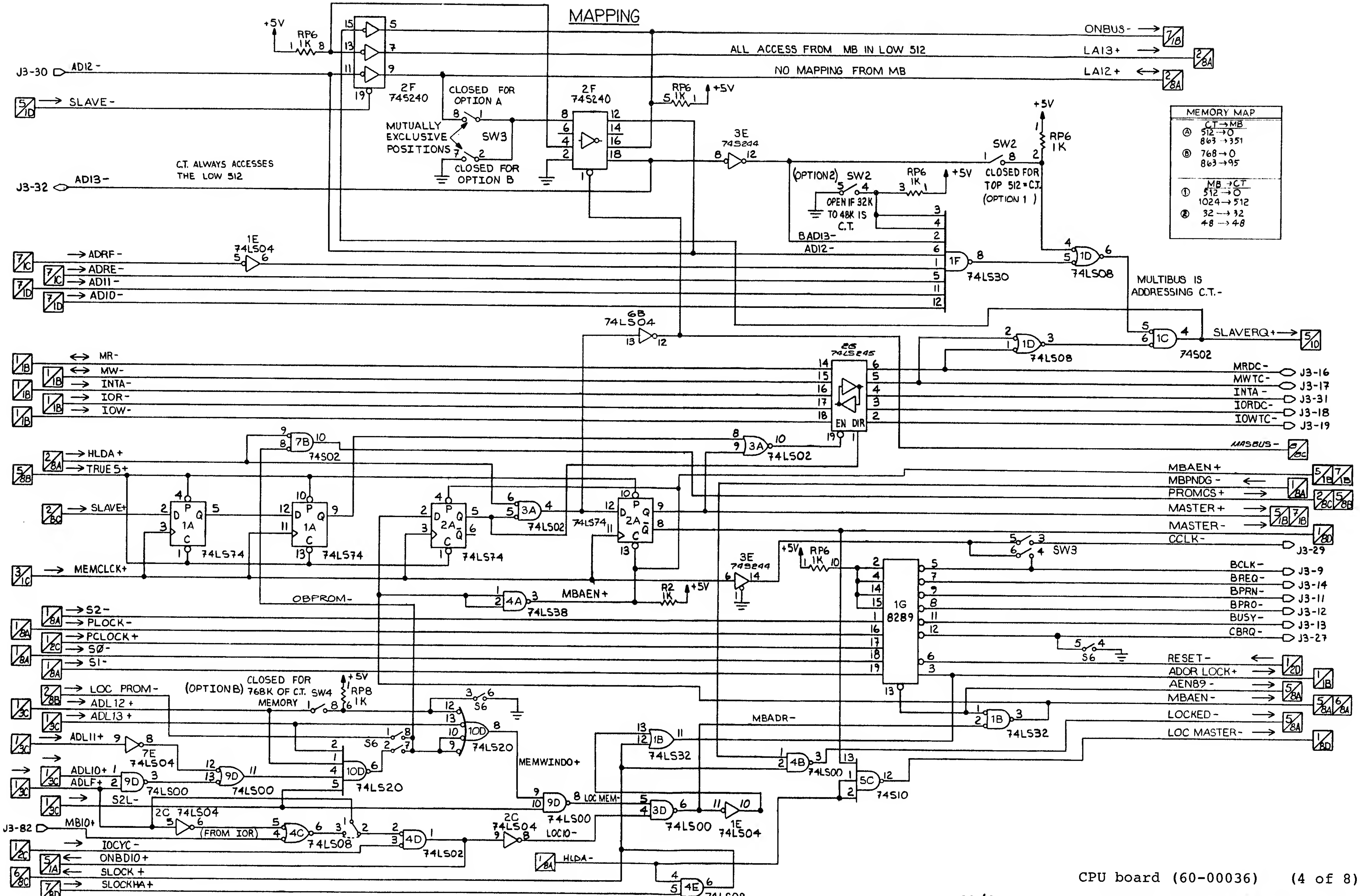
S2-	S1-	S0-	
0	0	0	INTA
0	0	1	IOR
0	1	0	IOW
0	1	1	HLT
1	0	0	FETCH
1	0	1	READ MEM DATA
1	1	0	WRITE MEM
1	1	1	PASSIVE

CPU board (60-00036) (1 of 8)

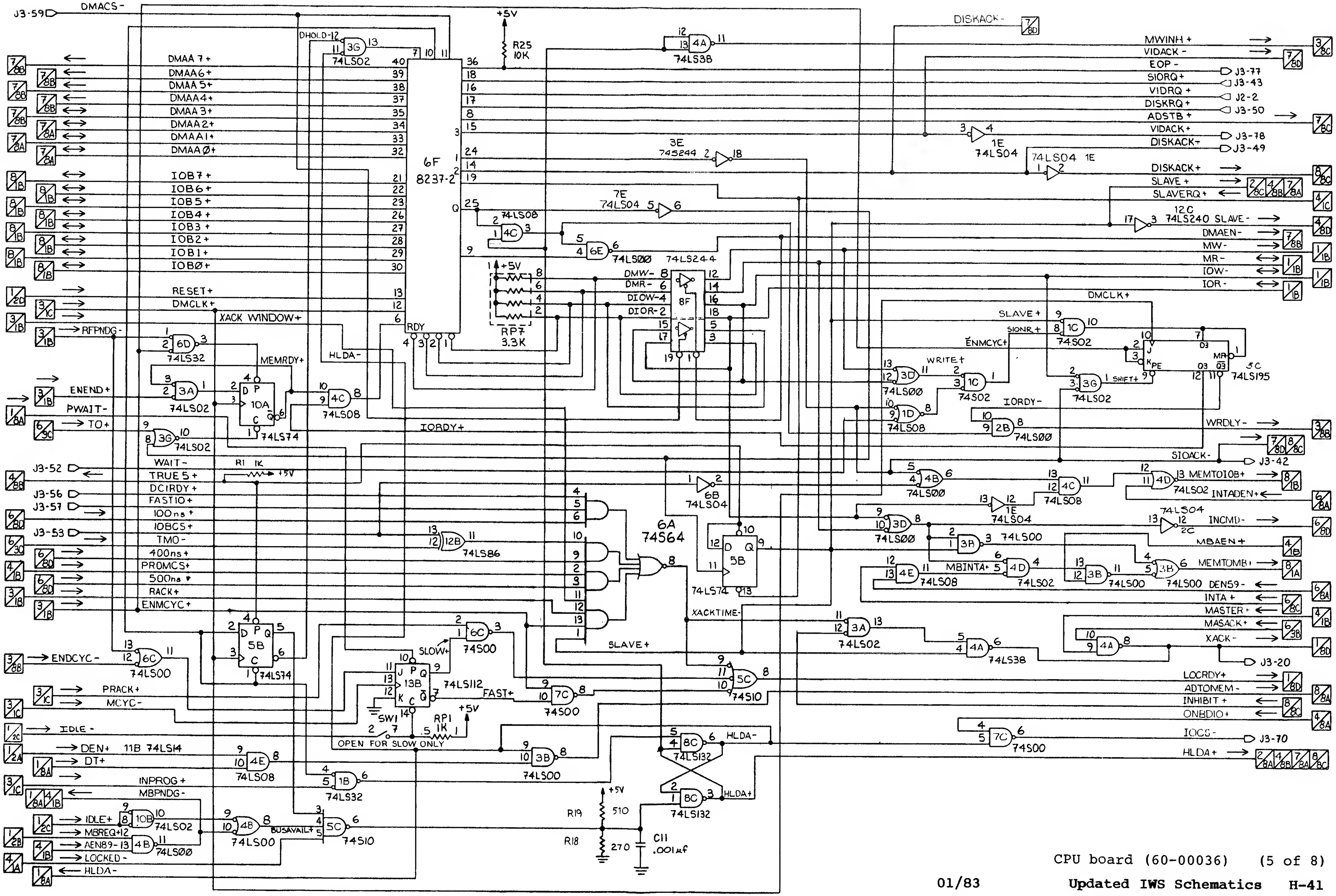

COLD+
HIP+
J2-23
CHECKP-
PRESELECT+
PROMCS+
PAREN+
J3-84
SLAVE+
MR+
ODDP+
J3-51
LOCPROM-
MR-
LOP+
J2-24
HLDA+
LBHEN+
RDHIPEA-
RDLOPEA-
J3-44
J3-47
LA10+-LA13+
14C
74LS244
13F
74S280
12B
74LS86
10C
74LS32
12C
74LS240
11C
74LS10
13C
74LS112
RP1
1K
TRUE+
+5V
9D
74LS00
11B
74LS14
13G
74S280
11F
74LS374
12F
74LS30
RP8
1K
LAF+
LA13+
LA12+
LA11+
LA10+
12D
74LS374
MUTUALLY
EXCLUSIVE
PROMAC+
SW5
CLOSED FOR
2716/2316
14F
2316
[2716]
2732
2332
2364
MEMF+
MEME+
MEMD+
MEMC+
MEMB+
MEMA+
MEM9+
MEM8+
LA1+
LA2+
LA3+
LA4+
LA5+
LA6+
LA7+
LA8+
LA9+
LAA+
LAB+
LAD+
LAC+
LAE+
LAF+
PROMEXDC-
J2-8
PERINT+
J3-79
LA0+
15F
MEM7+
MEM6+
MEM5+
MEM4+
MEM3+
MEM2+
MEM1+
MEM0+
LOCPROM-
12E
74LS374
LA7+
LA6+
LA5+
LA4+
LA3+
LA2+
LA1+
LA0+



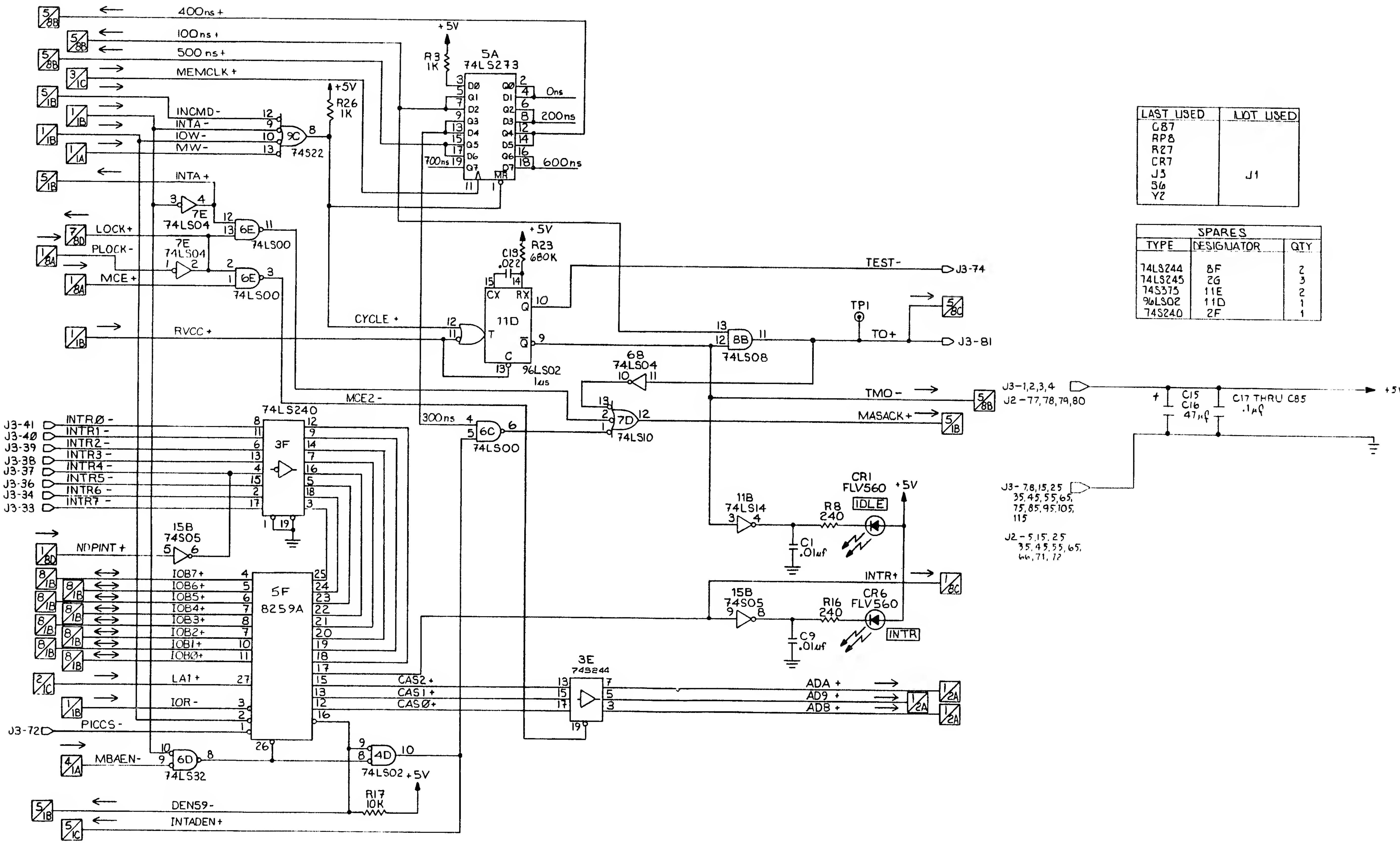
SW1
+5V
RP1 1K
OPEN: 8237 5 MHZ
CLOSED: 951 4 MHZ
TRUE3+
Y1 20 MHZ
R10 330
R9 330
C3 680 pf
C8 10 pf
C7
15A 74S04
14A 74S163
13A 74LS161
12A 74LS161
20MHZ+
2C 74LS04
MEMCLK+
C86 56pf
MEMCLK-
14C 74LS244
BMEMCLK+
J3-73
DMCLK+
78KHZ+
J2-13
PRESELECT+
MCYC-
6B 74LS04
74LS74
TP4
13B 74LS112
10B 74LS02
10A
RFTIME-
PRESELECT+
ENDCYC-
CYCLE REQ+
9C 74S22
R21 510
R20 510
C12 270 pf
START-
8C 74S132
ENMCYC+
9B 74LS32
CYCINPROG+
1B 74LS32
INPROG+
MR-
7C 74S00
MW-
6D 74LS32
FOR SLOW PROCESSOR ACCESSES
PRACK+
14B 74LS74
J3-80
MWINH+
WRDLY-
2B 74LS00
PRACKTIME-
TP3
8B 74LS08
11A 74S112
RFDONE+
RFDONE-
ENDCYC-
11B 74LS14
RFGO-
J2-9
J2-10
ENDCYC+
RFGO+
RFPNDG-
ENDCYC-
NORF-
ENEND+
7B 74S02
ENMCYC-
ENMCYC+
TP5
BENMCYC+
J2-75
XACK WINDOW+
CASTIME-
R4 270
ANYCYC+
7A 74S140
9A PE9828
8A PE9828
R5 270Ω
RACK+
RARAS-
J2-7
COLMPX-
J2-6
R6 240
R7 120
RFRAS+
DELAY FOR ADR BUFFERS



CPU board (60-00036) (4 of 8)

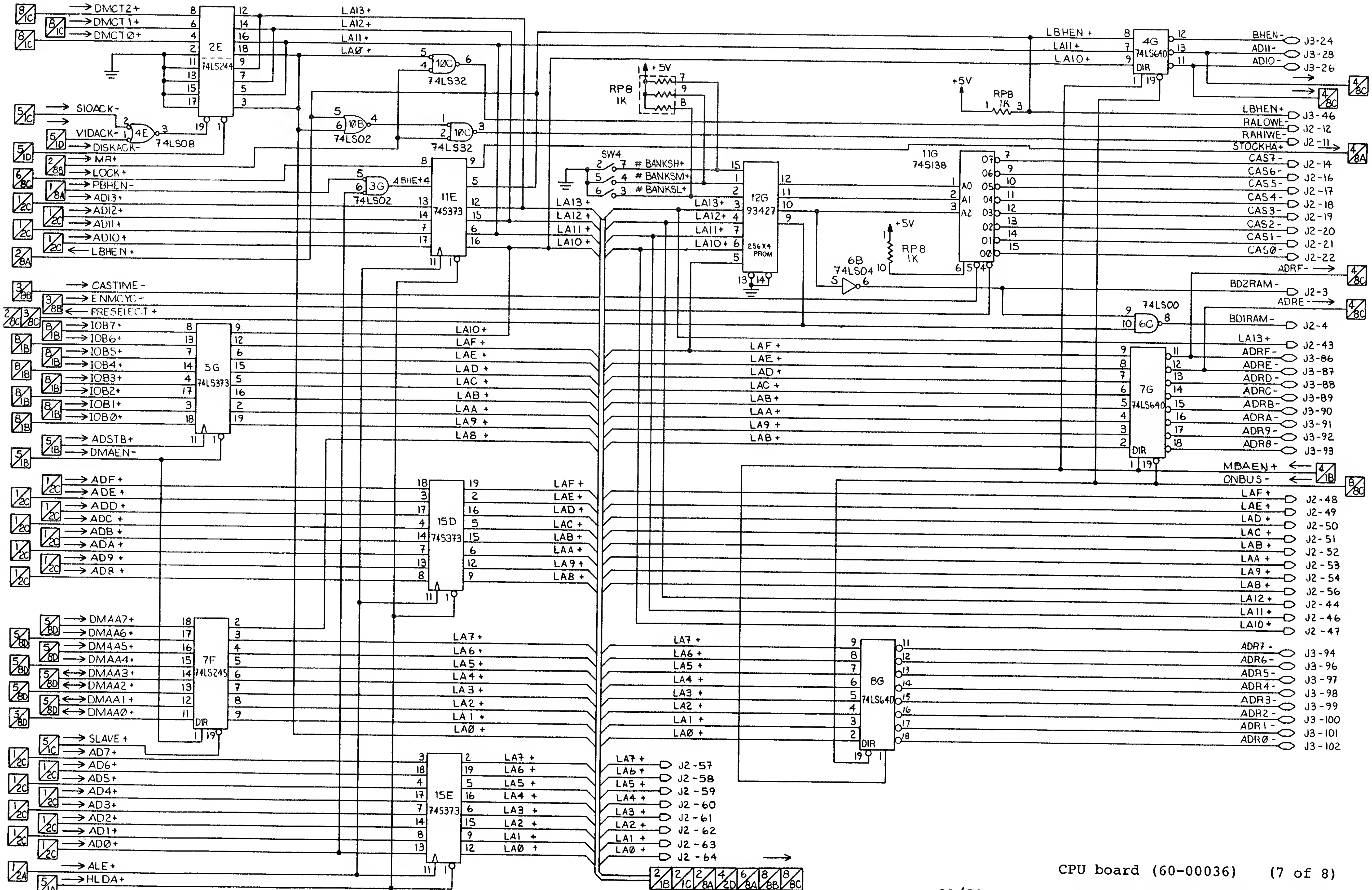


CPU board (60-00036) (5 of 8)

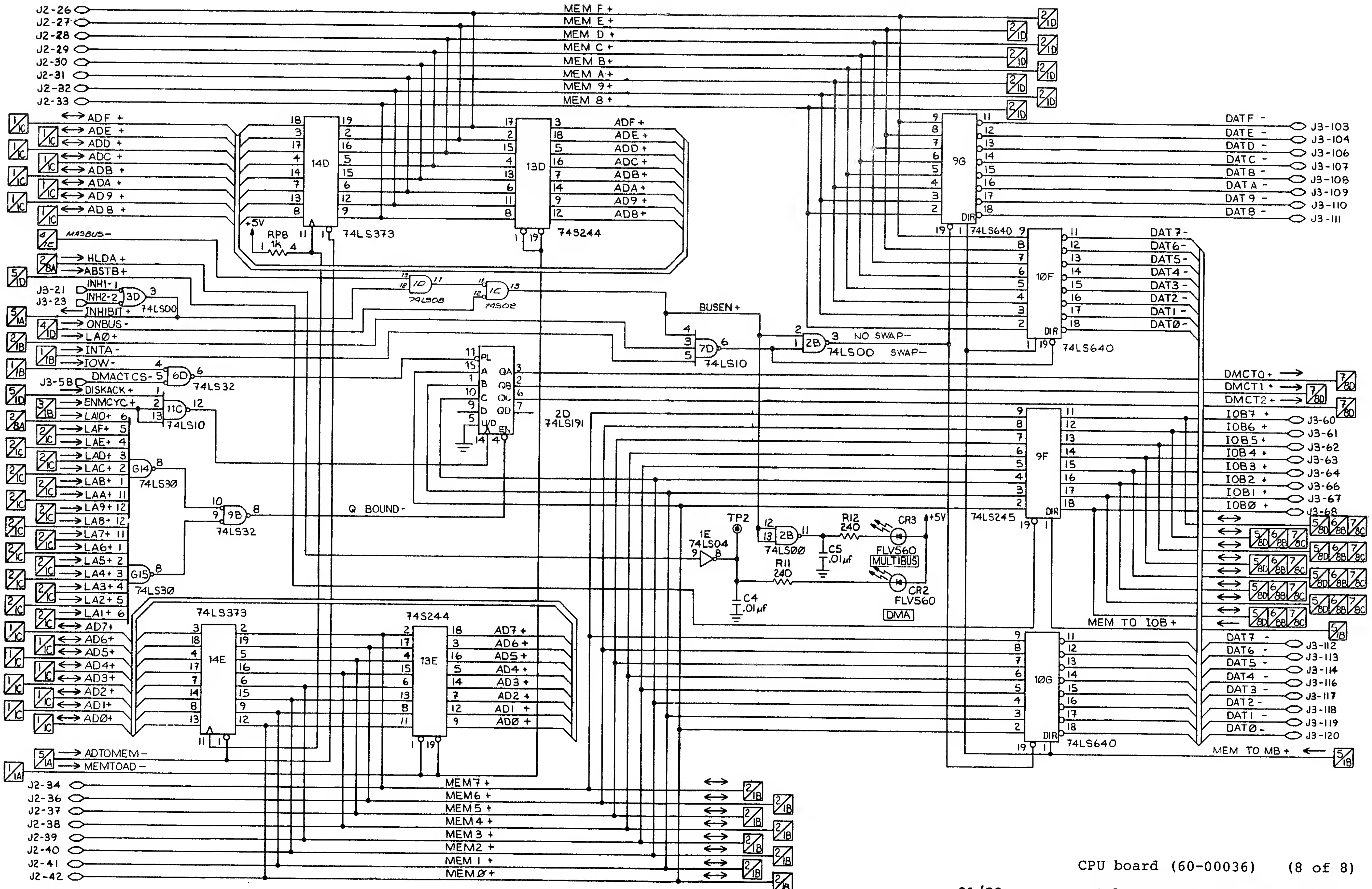


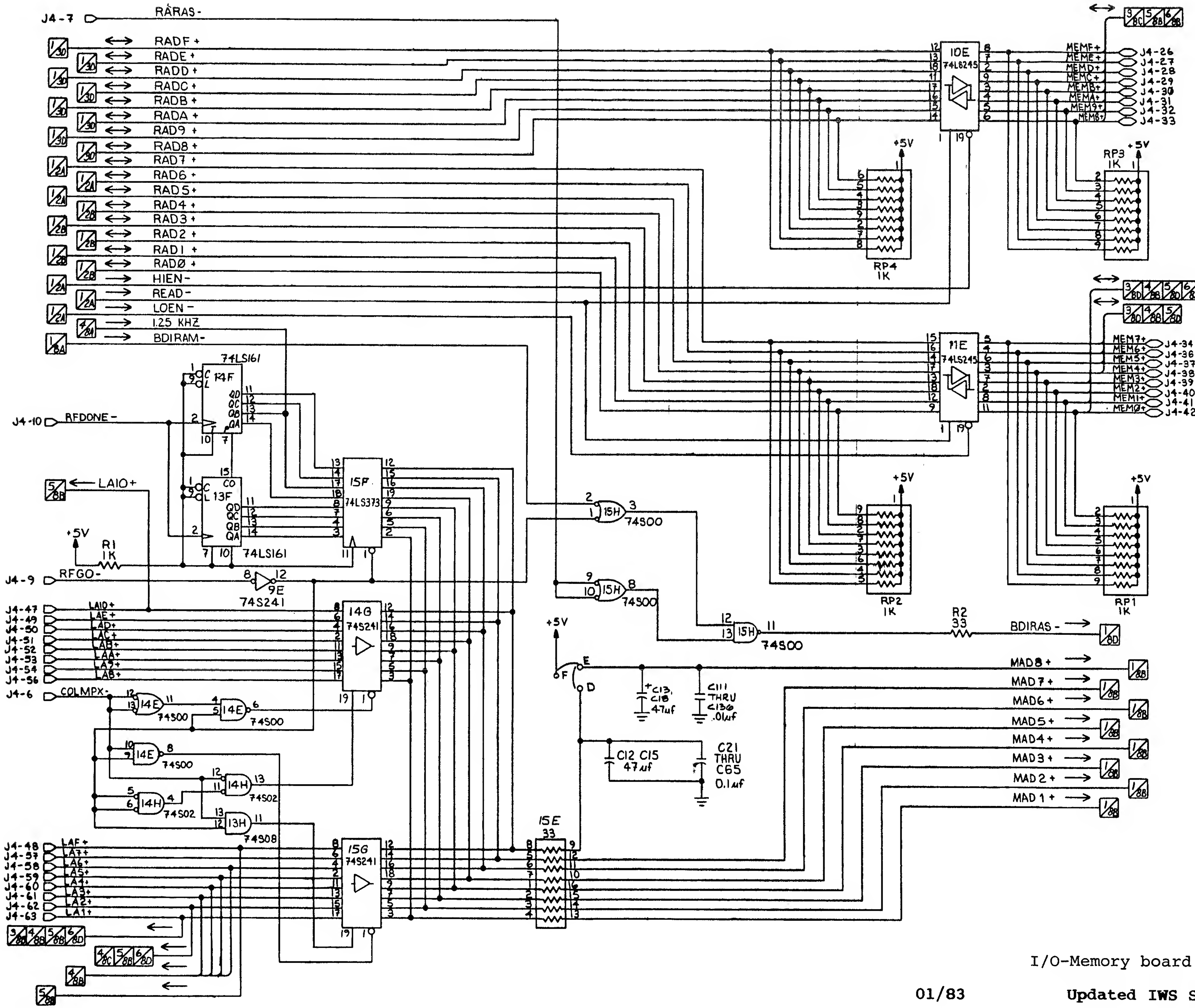
LAST USED	NOT USED
C87	
RP8	
R27	
CR7	
J3	J1
S6	
Y2	

SPARES		
TYPE	DESIGNATOR	QTY
74LS244	8F	2
74LS245	2G	3
74S375	11E	2
96LS02	11D	1
74S240	2F	1

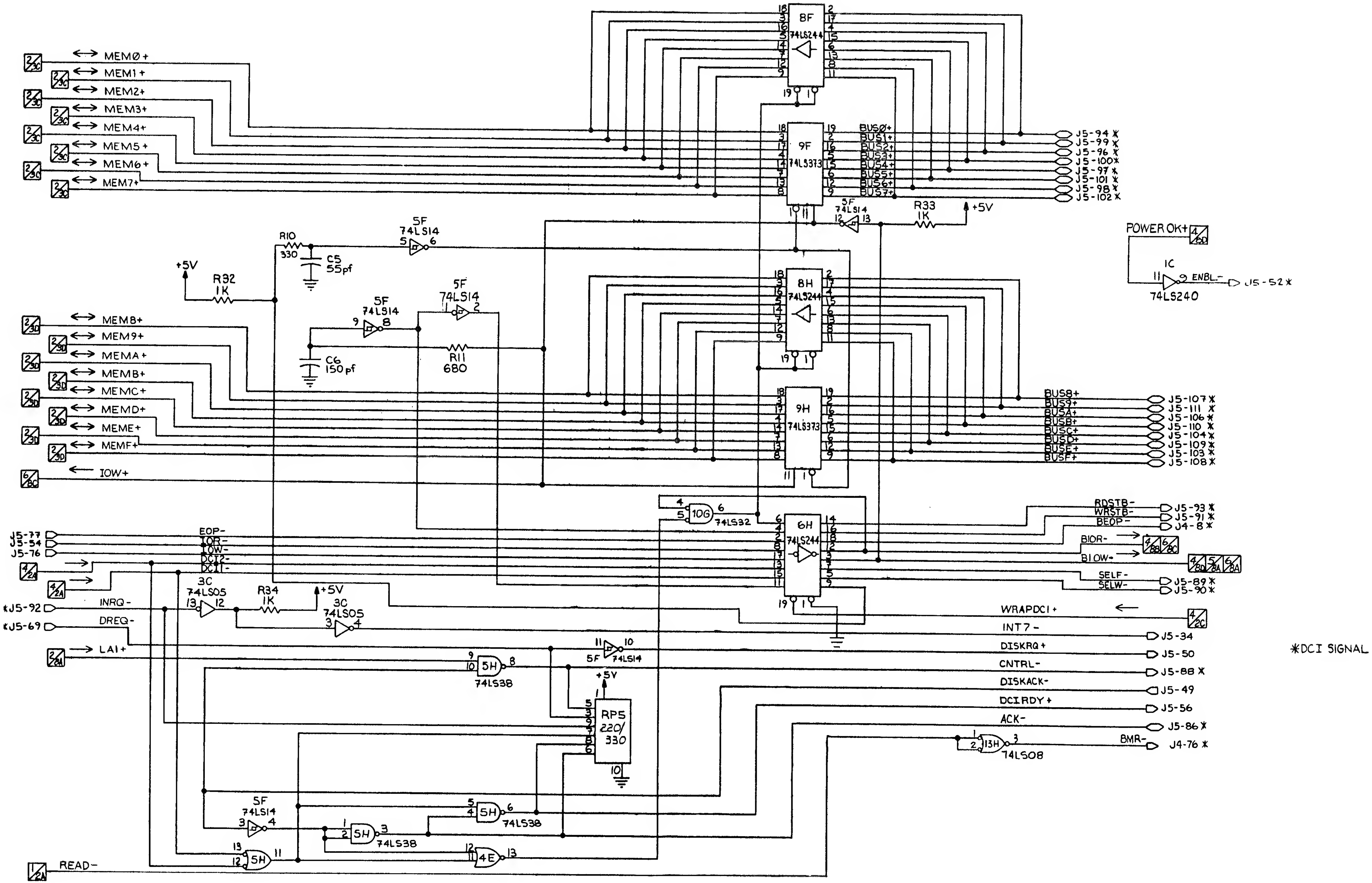


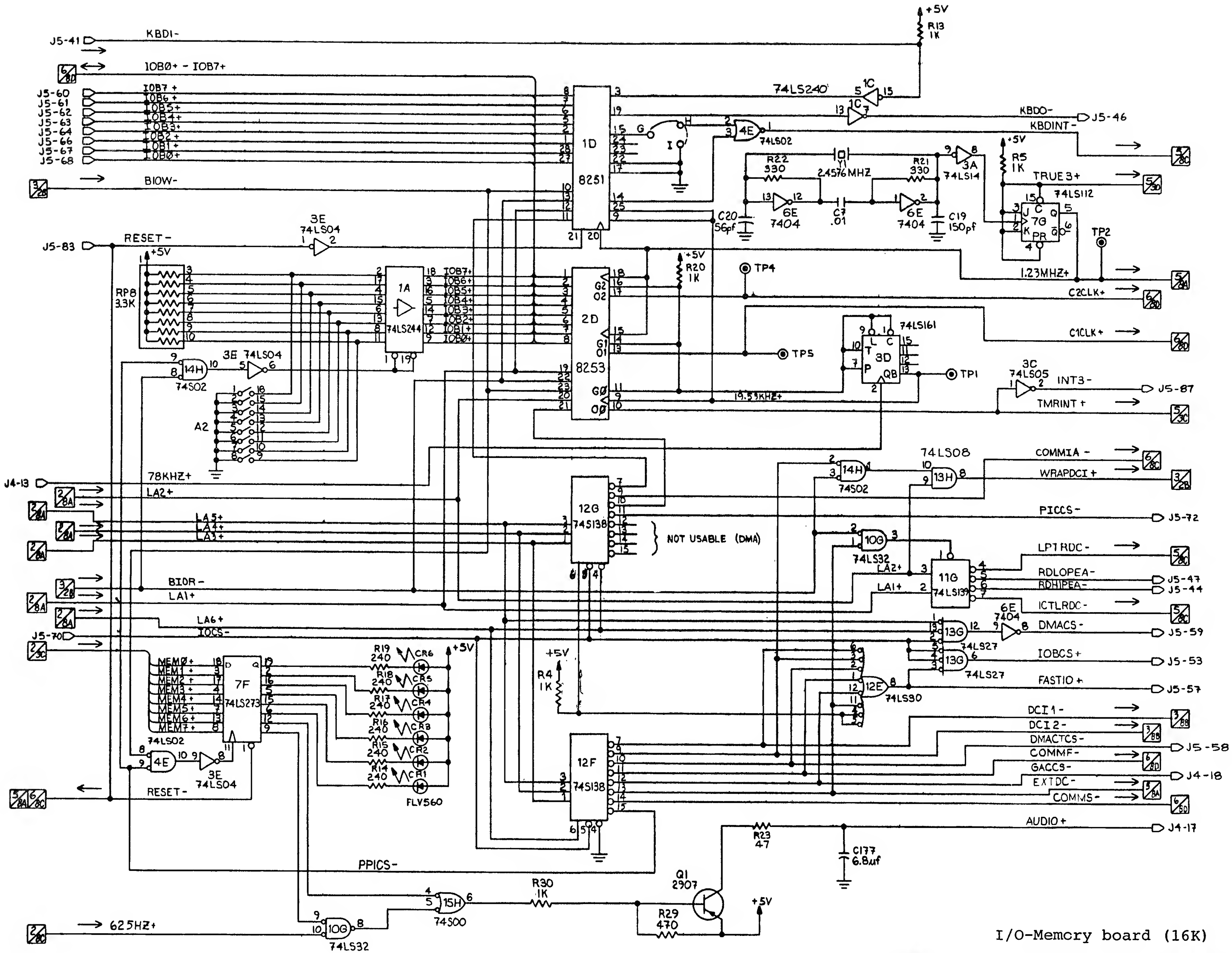
DMCT2+
DMCT1+
DMCTØ+
2E
74LS244
LA13+
LA12+
LA11+
LAØ+
10C
74LS32
SIOACK-
VIDACK-
DISKACK-
4E
74LS08
10B
74LS02
MR+
LOCK+
PBHEN-
AD13+
AD12+
AD11+
AD10+
LBHEN+
3G
74LS02
BHE+
11E
74S373
RP8
1K
+5V
SW4
BANKSH+
BANKSM+
BANKSL+
12G
93427
256X4 PROM
11G
74S138
6B
74LS04
LBHEN+
LA11+
LA10+
4G
74LS640
DIR
BHEN-
AD11-
AD10-
J3-24
J3-28
J3-26
RALOWE-
RAHIWE-
STOCKHA+
J3-46
J2-12
J2-11
CAS7-
CAS6-
CAS5-
CAS4-
CAS3-
CAS2-
CAS1-
CASØ-
J2-14
J2-16
J2-17
J2-18
J2-19
J2-20
J2-21
J2-22
ADRF-
BD2RAM-
J2-3
ADRE-
74LS00
6C
BDIRAM-
J2-4
CASTIME-
ENMCYC-
PRESELECT+
IOB7+
IOB6+
IOB5+
IOB4+
IOB3+
IOB2+
IOB1+
IOBØ+
5G
74LS373
ADSTB+
DMAEN-
LAF+
LAE+
LAD+
LAC+
LAB+
LAA+
LA9+
LA8+
7G
74LS640
ADRD-
ADRC-
ADRB-
ADRA-
ADR9-
ADR8-
J2-43
J3-86
J3-87
J3-88
J3-89
J3-90
J3-91
J3-92
J3-93
MBAEN+
ONBUS-
ADF+
ADE+
ADD+
ADC+
ADB+
ADA+
AD9+
AD8+
15D
74S373
J2-48
J2-49
J2-50
J2-51
J2-52
J2-53
J2-54
J2-56
J2-44
J2-46
J2-47
DMAA7+
DMAA6+
DMAA5+
DMAA4+
DMAA3+
DMAA2+
DMAA1+
DMAAØ+
7F
74LS245
LA7+
LA6+
LA5+
LA4+
LA3+
LA2+
LA1+
LAØ+
8G
74LS640
ADR7-
ADR6-
ADR5-
ADR4-
ADR3-
ADR2-
ADR1-
ADRØ-
J3-94
J3-96
J3-97
J3-98
J3-99
J3-100
J3-101
J3-102
SLAVE+
AD7+
AD6+
AD5+
AD4+
AD3+
AD2+
AD1+
ADØ+
15E
74S373
J2-57
J2-58
J2-59
J2-60
J2-61
J2-62
J2-63
J2-64
ALE+
HLDA+


J2-26
J2-27
J2-28
J2-29
J2-30
J2-31
J2-32
J2-33
MEM F +
MEM E +
MEM D +
MEM C +
MEM B +
MEM A +
MEM 9 +
MEM 8 +
ADF +
ADE +
ADD +
ADC +
ADB +
ADA +
AD9 +
AD8 +
MASBUS-
HLDA +
ABSTB +
J3-21
J3-23
INH1-1
INH2-2
3D
74LS00
INHIBIT +
ONBUS -
LAØ +
INTA -
IOW -
J3-58
DMACTCS-
DISKACK +
6D
74LS32
ENMCYC +
11C
74LS10
LAIO+
LAF+
LAE+
LAD+
LAC+
LAB+
LAA+
LA9+
LA8+
LA7+
LA6+
LA5+
LA4+
LA3+
LA2+
LA1+
G14
74LS30
9B
74LS32
G15
74LS30
Q BOUND-
14D
74LS373
13D
74S244
+5V
RP8
1k
1D
74LS08
1C
74S02
BUSEN +
7D
74LS10
2B
74LS00
NO SWAP-
SWAP-
2D
74LS191
PL
QA
QB
QC
QD
U/D
EN
9G
74LS640
10F
74LS640
DIR
DATF -
DATE -
DATD -
DATC -
DATB -
DATA -
DAT9 -
DAT8 -
J3-103
J3-104
J3-106
J3-107
J3-108
J3-109
J3-110
J3-111
DAT7-
DAT6-
DAT5-
DAT4-
DAT3-
DAT2-
DAT1-
DATØ-
DMCTO +
DMCT1 +
DMCT2 +
9F
74LS245
IOB7 +
IOB6 +
IOB5 +
IOB4 +
IOB3 +
IOB2 +
IOB1 +
IOBØ +
J3-60
J3-61
J3-62
J3-63
J3-64
J3-66
J3-67
J3-68
TP2
1E
74LS04
2B
74LS00
R12
240
R11
240
C5
.01µf
C4
.01µf
CR3
FLV560
MULTIBUS
CR2
FLV560
DMA
MEM TO IOB +
10G
74LS640
DAT7 -
DAT6 -
DAT5 -
DAT4 -
DAT3 -
DAT2 -
DAT1 -
DATØ -
J3-112
J3-113
J3-114
J3-116
J3-117
J3-118
J3-119
J3-120
MEM TO MB +
AD7+
AD6+
AD5+
AD4+
AD3+
AD2+
AD1+
ADØ+
14E
74LS373
13E
74S244
ADTOMEM -
MEMTOAD -
J2-34
J2-36
J2-37
J2-38
J2-39
J2-40
J2-41
J2-42
MEM7 +
MEM6 +
MEM5 +
MEM4 +
MEM3 +
MEM2 +
MEM 1 +
MEMØ +

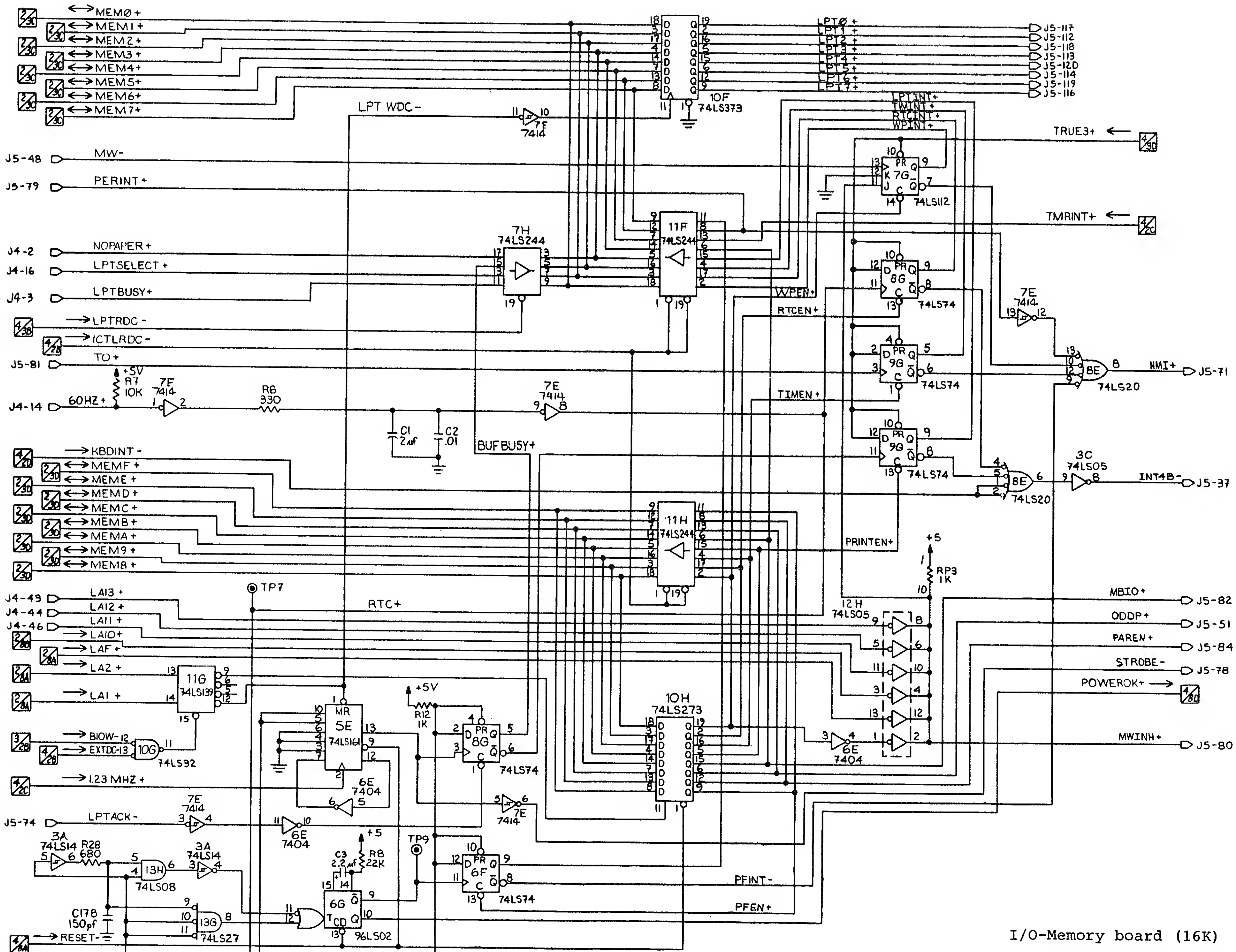


I/O-Memory board (16K) (2 of 6)

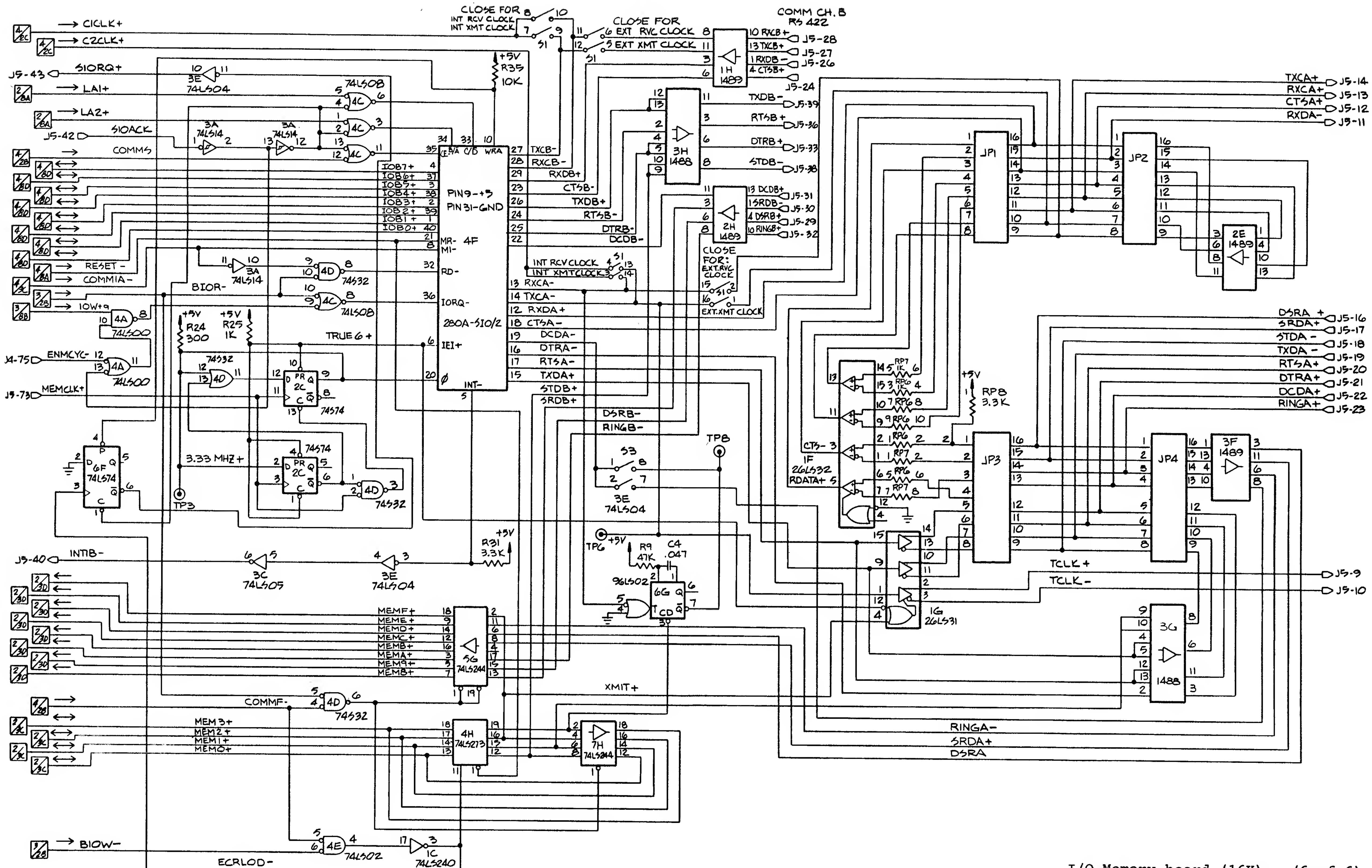

8F
74LS244
9F
74LS373
8H
74LS244
9H
74LS373
6H
74LS244
MEMØ+
MEM1+
MEM2+
MEM3+
MEM4+
MEM5+
MEM6+
MEM7+
MEM8+
MEM9+
MEMA+
MEMB+
MEMC+
MEMD+
MEME+
MEMF+
IOW+
BUSØ+
BUS1+
BUS2+
BUS3+
BUS4+
BUS5+
BUS6+
BUS7+
BUS8+
BUS9+
BUSA+
BUSB+
BUSC+
BUSD+
BUSE+
BUSF+
J5-94 *
J5-99 *
J5-96 *
J5-100 *
J5-97 *
J5-101 *
J5-98 *
J5-102 *
J5-107 *
J5-111 *
J5-106 *
J5-110 *
J5-104 *
J5-109 *
J5-103 *
J5-108 *
R10
330
C5
55pf
R32
1K
+5V
C6
150pf
R11
680
5F
74LS14
R33
1K
POWER OK+
1C
74LS240
ENBL-
J5-52 *
10G
74LS32
RDSTB-
WRSTB-
BEOP-
J5-93 *
J5-91 *
J4-8 *
BIOR-
BIOW-
SELF-
SELW-
J5-89 *
J5-90 *
J5-77
J5-54
J5-76
EOP-
IOR-
IOW-
DCI2-
DCI1-
*J5-92
INRQ-
*J5-69
DREQ-
3C
74LS05
R34
1K
WRAPDCI+
INT7-
J5-34
LAI+
DISKRQ+
J5-50
CNTRL-
J5-88 *
DISKACK-
J5-49
DCIRDY+
J5-56
ACK-
J5-86 *
5H
74LS38
RP5
220/
330
13H
74LS08
BMR-
J4-76 *
4E
READ-
*DCI SIGNAL



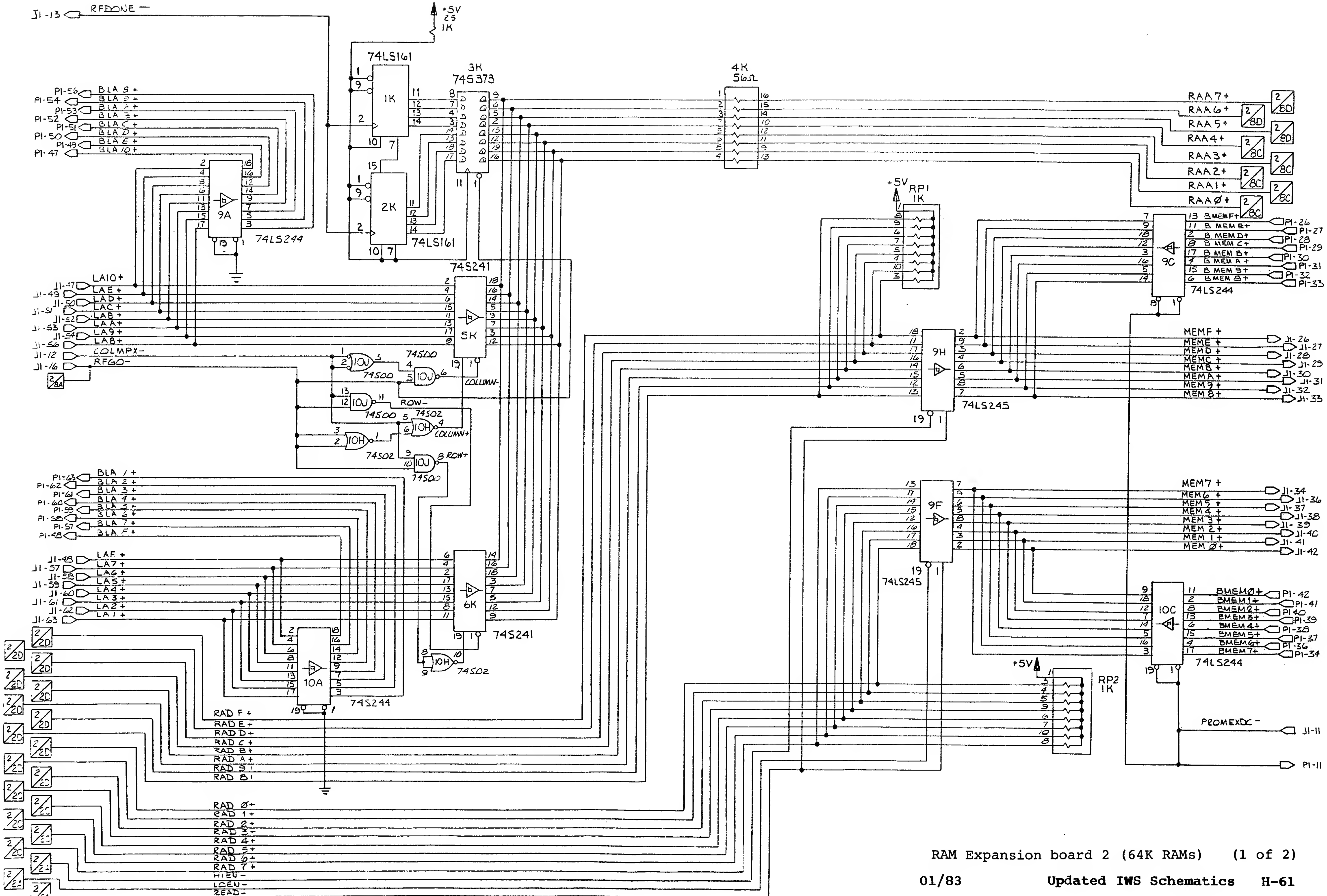
I/O-Memory board (16K) (4 of 6)



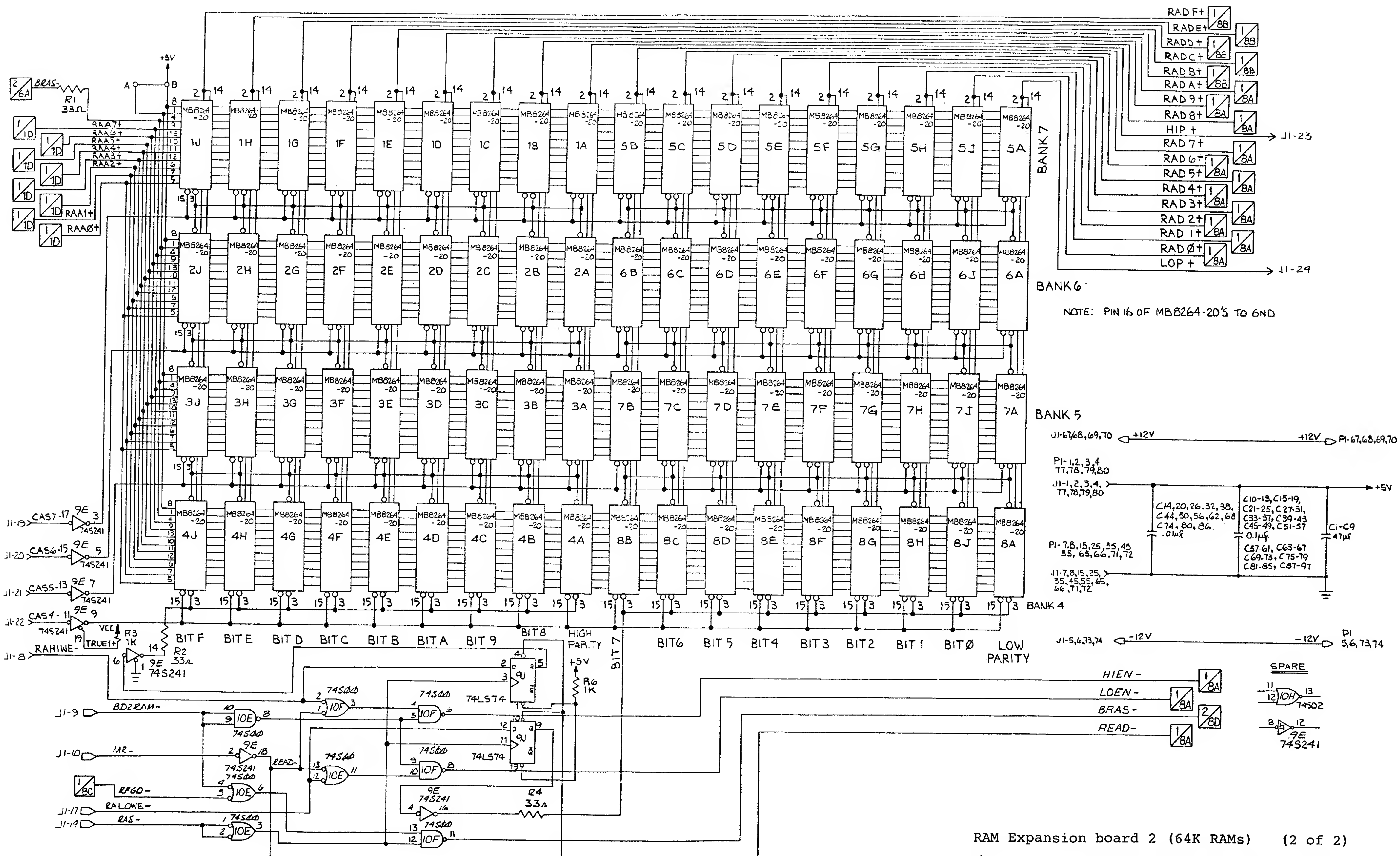
I/O-Memory board (16K) (5 of 6)



I/O-Memory board (16K) (6 of 6)



RAM Expansion board 2 (64K RAMs) (1 of 2)



RAM Expansion board 2 (64K RAMs) (2 of 2)

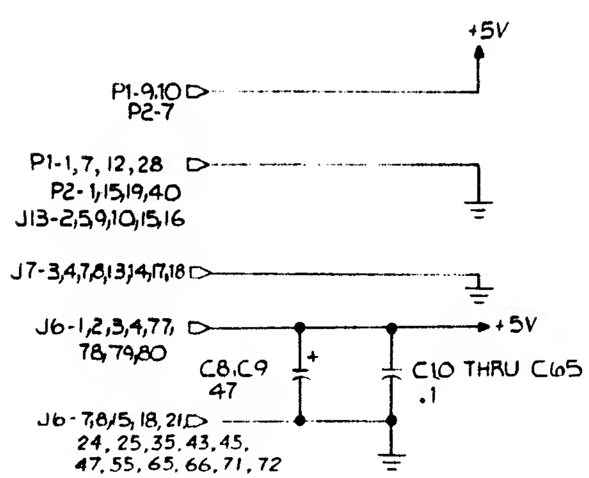
NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+8, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

SPARE GATES		
TYPE	REF. DESIGNATORS	QTY.
74LS32	1C	2
74LS86	1D	1
74LS244	9G	3
74LS244	11G	5
74LS244	13D	2

REF. DESIGNATORS	
LAST USED	NOT USED
P2	
J13	
G2	
C65	C1 THRU C4
RP9	
R28	R22
Q2	



P1

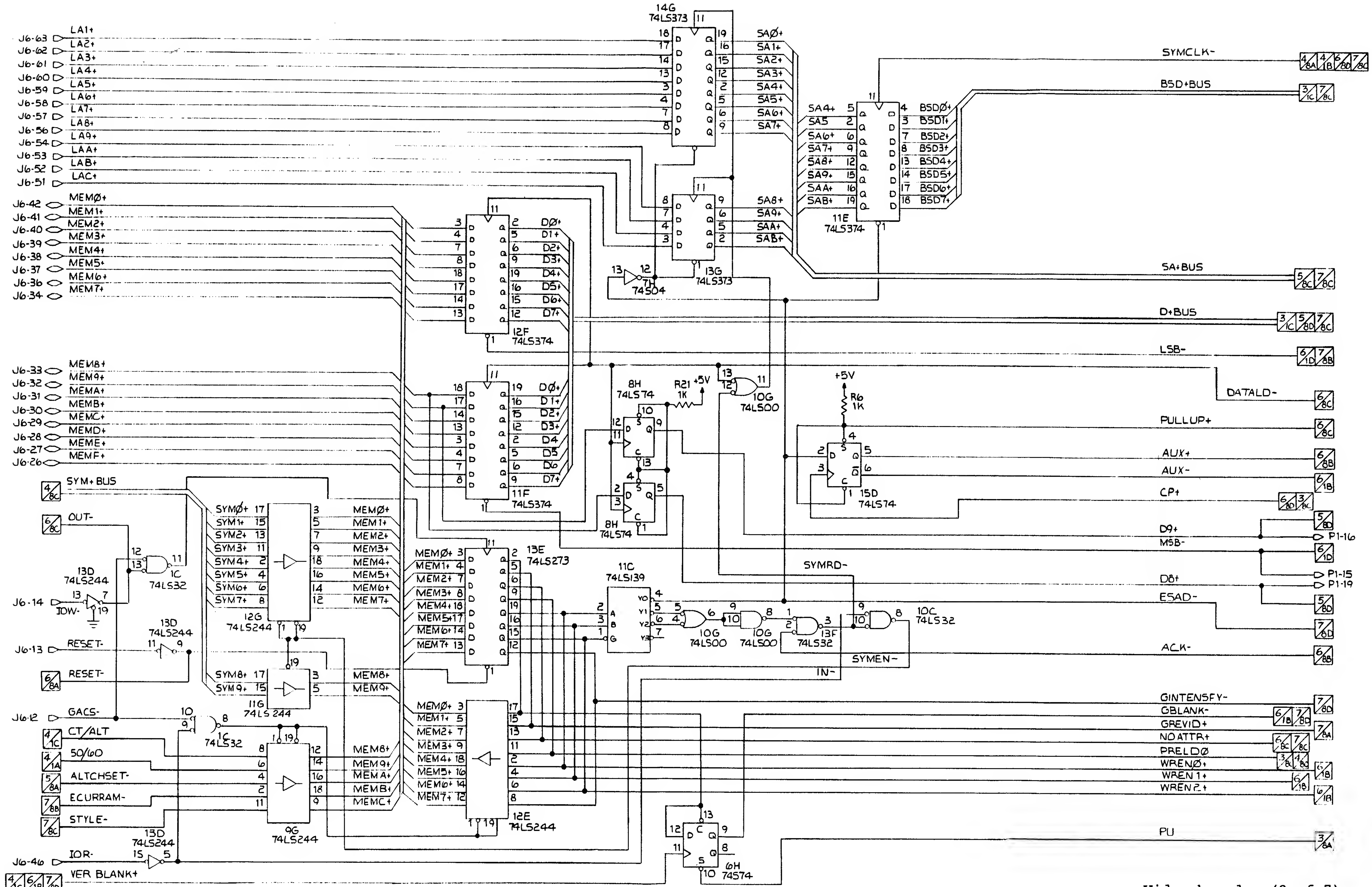
Pin	Signal
1	GND
2	SYMWR
3	CURSORWR -
4	STYLEWR -
5	HOLDOFF -
6	BLATWR -
7	GND
8	ALATWR-
9	Vcc
10	Vcc
11	ESAD-
12	GND
13	SELA +
14	HORBLANK +
15	MSB -
16	D9 +
17	NOATTR +
18	SYMCLK-
19	D8 +
20	D4 +
21	DØ +
22	D5 +
23	D1 +
24	D6 +
25	D2 +
26	D7 +
27	D3 +
28	GND
29	SAØ +
30	SA1 +
31	SA2 +
32	SA3 +
33	SA4 +
34	SA5 +
35	SA6 +
36	SA7 +
37	SA8 +
38	SAA +
39	SA9 +
40	SAB +

P2

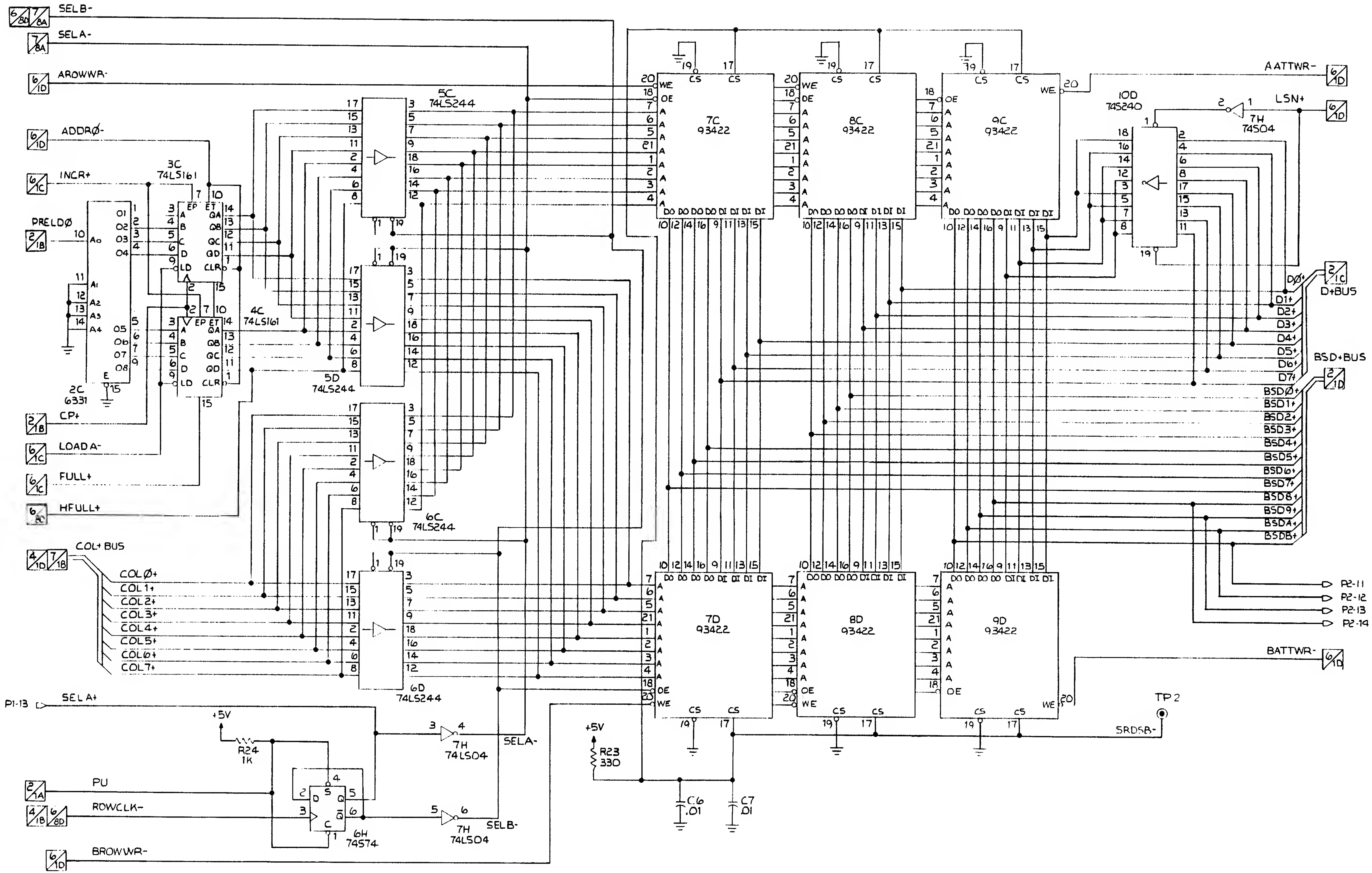
Pin	Signal
1	GND
2	UNDERLINE -
3	CURSOR -
4	ATTØ -
5	ATT2 -
6	VERBLANKEN +
7	Vcc
8	ECURRAM
9	ATT1 -
10	ATT3 -
11	BSDB +
12	BSDA +
13	BSD9 +
14	BSD8 +
15	GND
16	EPXCLK +
17	HPXCLK +
18	ESYMCLK -
19	GND
20	B1
21	B2
22	LLINE
23	T +
24	P +
25	ALTCHSET -
26	STYLE -
27	DLLC -
28	SYMØ +
29	SYM1 +
30	SYM2 +
31	SYM3 +
32	SYM4 +
33	SYM5 +
34	SYM6 +
35	SYM7 +
36	SYM8 +
37	SYM9 +
38	ESI +
39	CVIDEO -
40	GND

J7

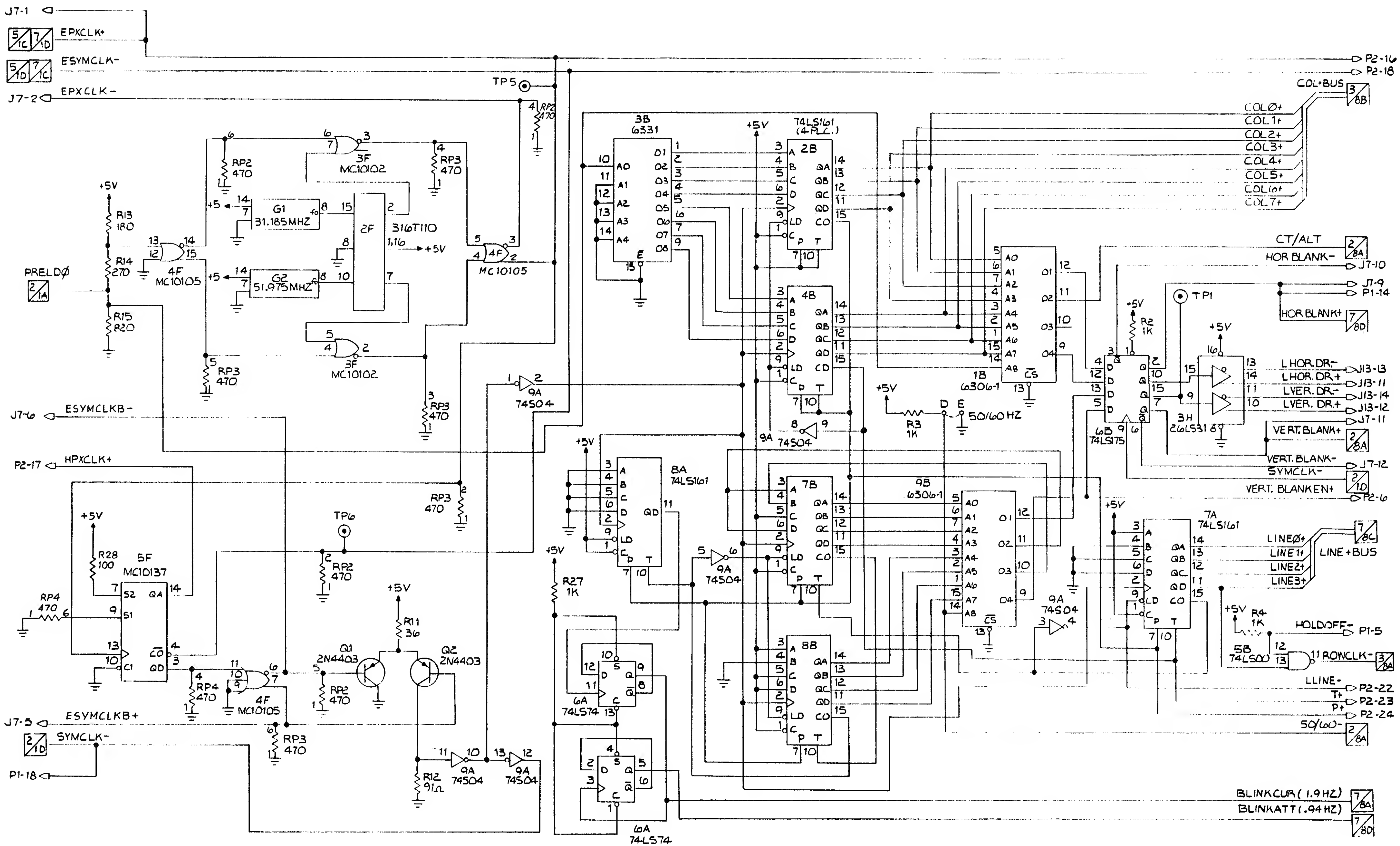
Signal	Pin	Pin	Signal
EPXCLK +	1	2	EPXCLK -
GND	3	4	GND
ESYMCLKB +	5	6	ESYMCLKB -
GND	7	8	GND
HORBLANK +	9	10	HORBLANK -
VERTBLANK +	11	12	VERTBLANK -
GND	13	14	GND
	15	16	HBVIDEO +
GND	17	18	GND
	19	20	AUX VIDEO A

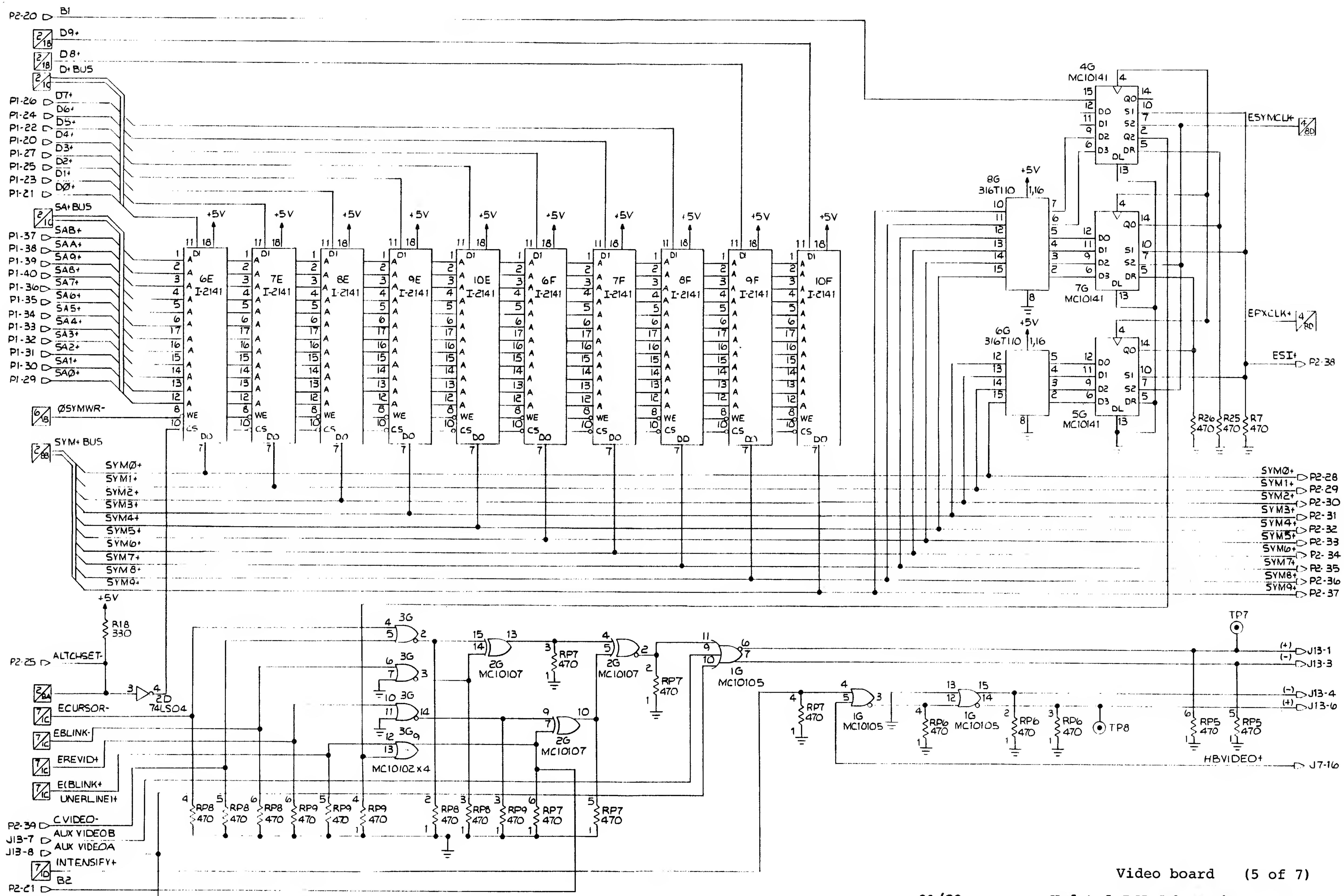


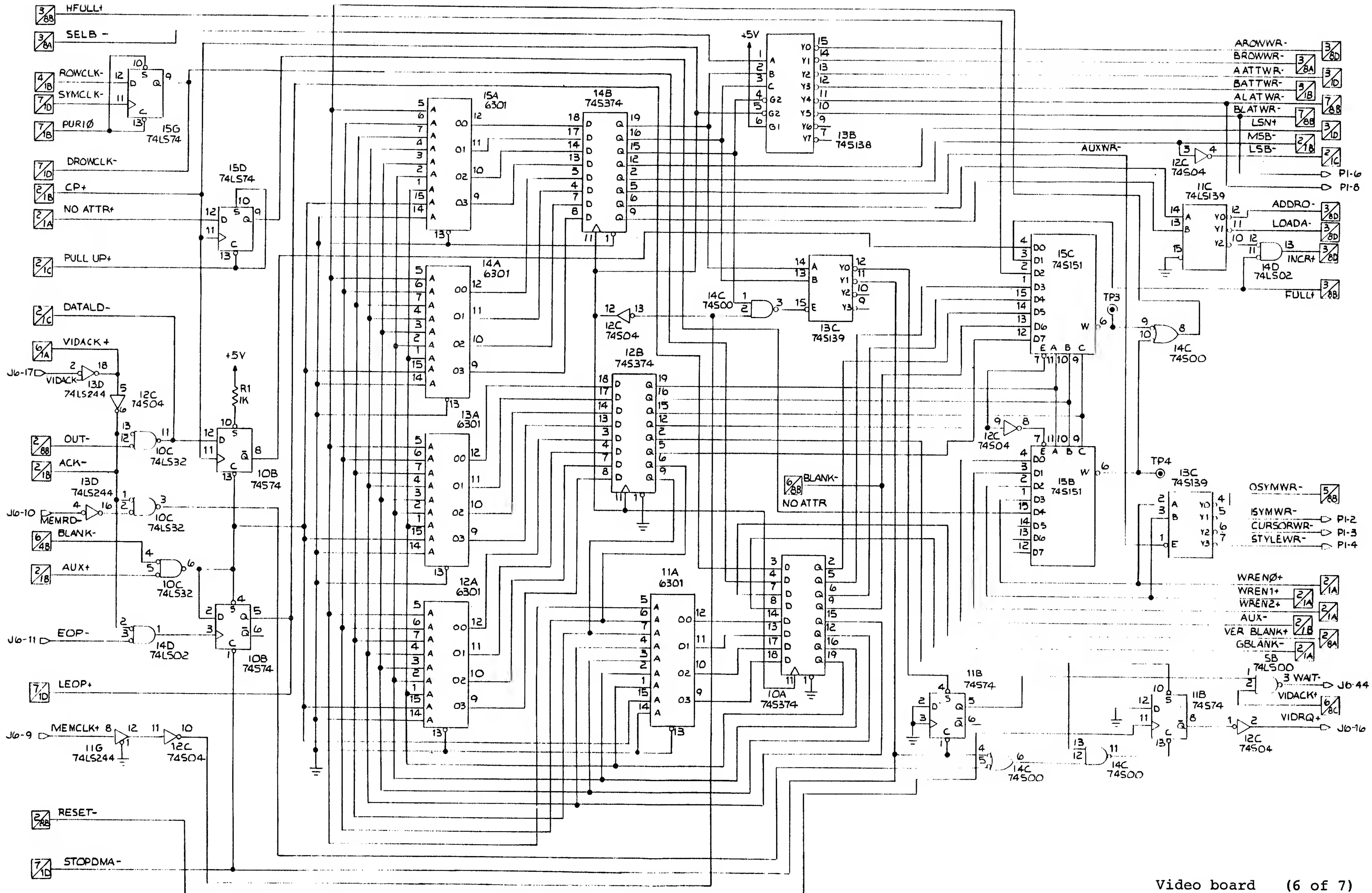
Video board (2 of 7)

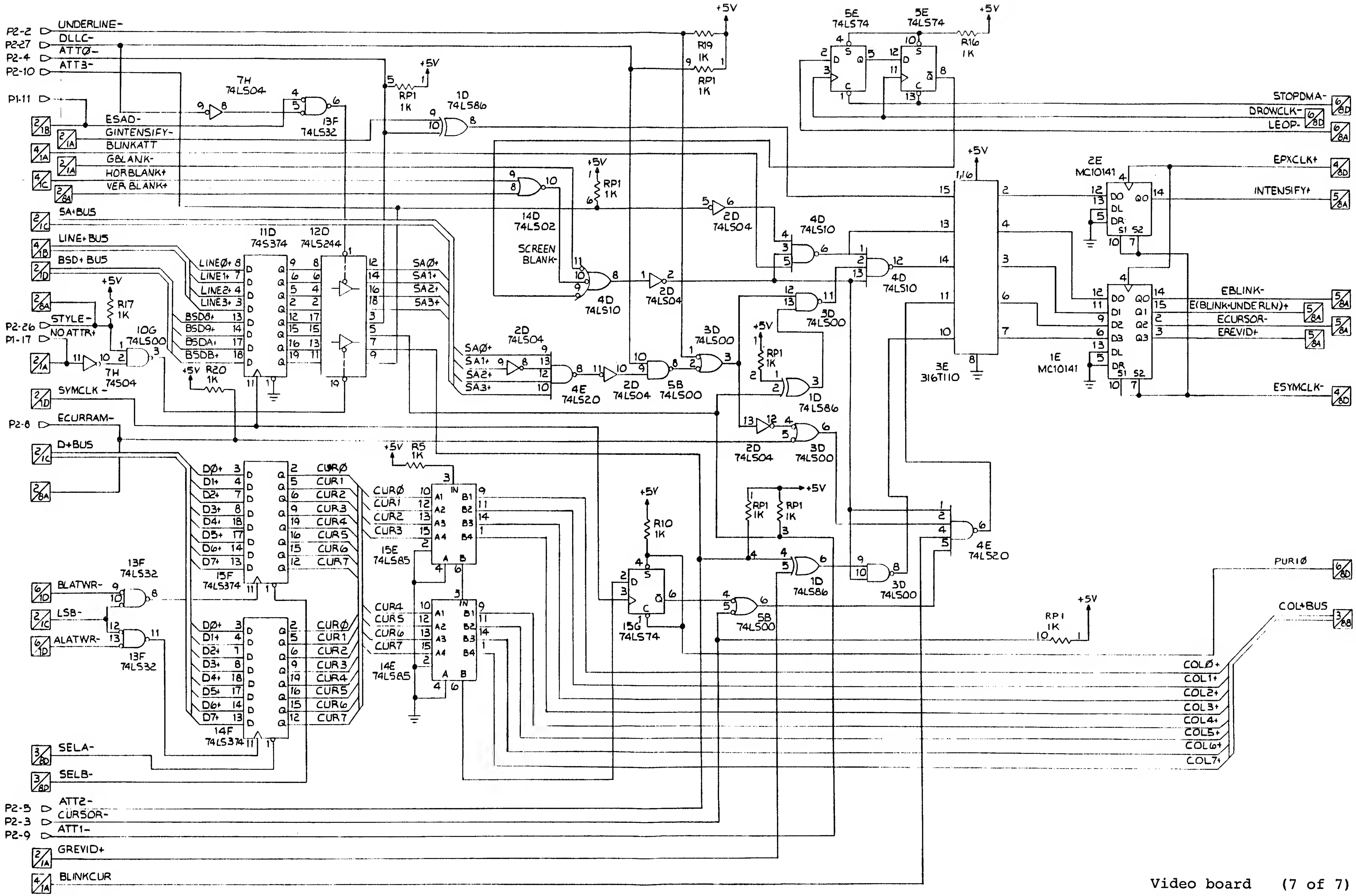


SELB-
SELA-
AROWWR-
ADDRØ-
INCR+
PRELDØ
CP+
LOADA-
FULL+
HFULL+
COL+ BUS
COLØ+
COL1+
COL2+
COL3+
COL4+
COL5+
COL6+
COL7+
SEL A+
P1-13
+5V
R24 1K
PU
ROWCLK-
BROWWR-
6H 74S74
7H 74LS04
SELA-
SELB-
2C 6331
3C 74LS161
4C 74LS161
5C 74LS244
5D 74LS244
6C 74LS244
6D 74LS244
7C 93422
8C 93422
9C 93422
7D 93422
8D 93422
9D 93422
10D 74S240
7H 74S04
AATTWR-
LSN+
D+BUS
BSD+BUS
BATTWR-
TP2
SRDSB-
R23 330
C6 .01
C7 .01
P2-11
P2-12
P2-13
P2-14

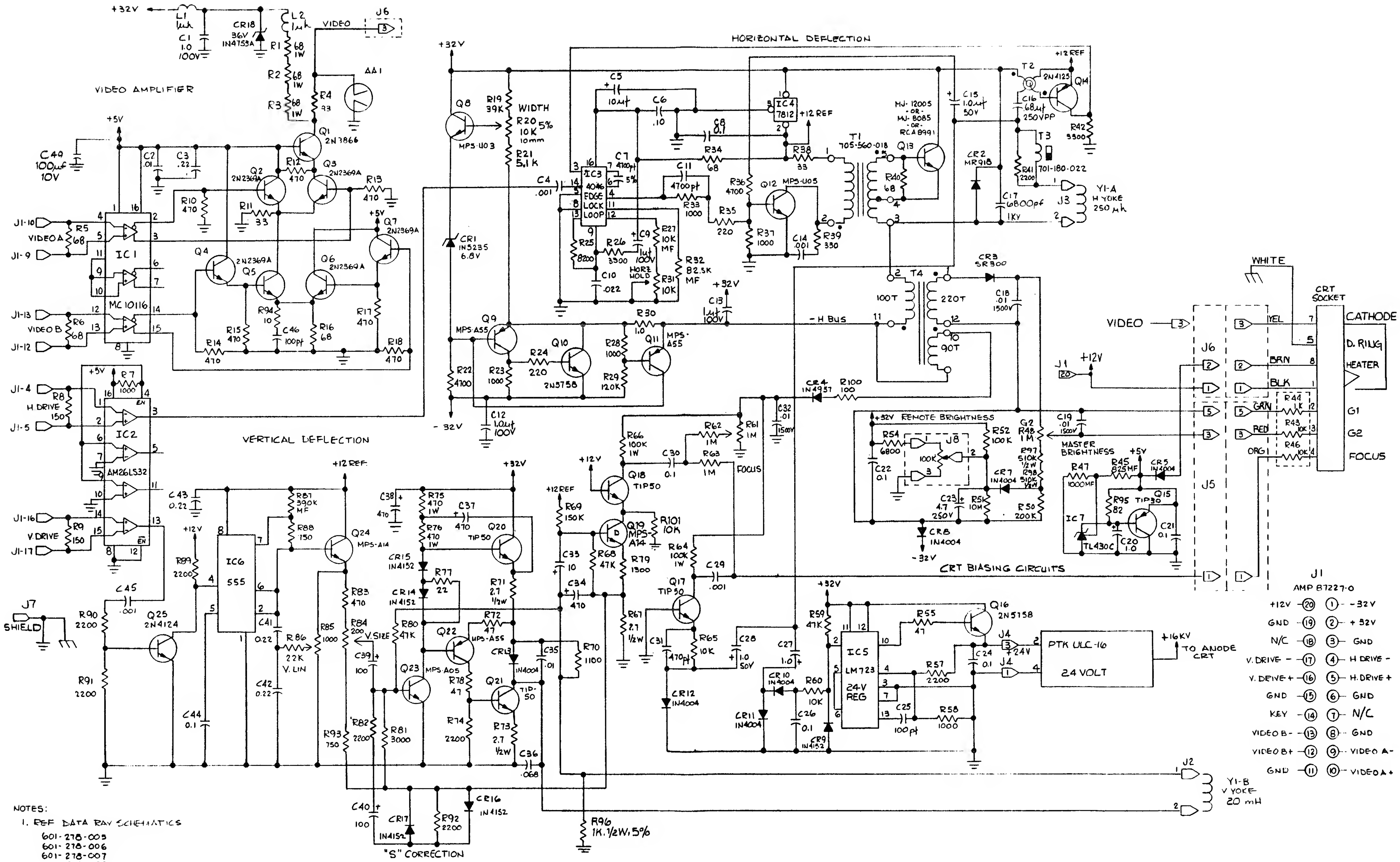

J7-1
EPXCLK+
ESYMCLK-
J7-2
EPXCLK-
TP5
P2-16
P2-18
COL+BUS
COLØ+
COL1+
COL2+
COL3+
COL4+
COL5+
COL6+
COL7+
3B
6331
74LS161
(4-PLC.)
2B
4B
+5V
3F
MC10102
G1
31.185 MHZ
G2
51.975 MHZ
2F
316T110
R13
180
R14
270
R15
820
PRELDØ
4F
MC10105
RP2
470
RP3
470
1B
6306-1
CT/ALT
HOR BLANK-
J7-10
J7-9
P1-14
TP1
HOR BLANK+
6B
74LS175
3H
26LS31
LHOR.DR-
LHOR.DR+
LVER.DR-
LVER.DR+
J13-13
J13-11
J13-14
J13-12
J7-11
VERT.BLANK+
VERT.BLANK-
J7-12
SYMCLK-
VERT.BLANKEN+
P2-6
R3
1K
50/60 HZ
9A
74S04
J7-6
ESYMCLKB-
P2-17
HPXCLK+
8A
74LS161
7B
9B
6306-1
7A
74LS161
LINEØ+
LINE1+
LINE2+
LINE3+
LINE+BUS
5F
MC10137
R28
100
RP4
470
TP6
Q1
2N4403
Q2
2N4403
R11
36
R12
91Ω
R27
1K
6A
74LS74
8B
R4
1K
HOLDOFF-
P1-5
5B
74LS00
ROWCLK-
LLINE-
T+
P+
P2-22
P2-23
P2-24
50/60-
J7-5
ESYMCLKB+
SYMCLK-
P1-18
BLINKCUR(1.9HZ)
BLINKATT(.94HZ)


P2-20 B1
D9+
D8+
D+BUS
P1-26 D7+
P1-24 D6+
P1-22 D5+
P1-20 D4+
P1-27 D3+
P1-25 D2+
P1-23 D1+
P1-21 DØ+
SA+BUS
P1-37 SAB+
P1-38 SAA+
P1-39 SA9+
P1-40 SA8+
P1-36 SA7+
P1-35 SA6+
P1-34 SA5+
P1-33 SA4+
P1-32 SA3+
P1-31 SA2+
P1-30 SA1+
P1-29 SAØ+
ØSYMWR-
SYM+BUS
SYMØ+
SYM1+
SYM2+
SYM3+
SYM4+
SYM5+
SYM6+
SYM7+
SYM8+
SYM9+
+5V
6E I-2141
7E I-2141
8E I-2141
9E I-2141
10E I-2141
6F I-2141
7F I-2141
8F I-2141
9F I-2141
10F I-2141
4G MC10141
8G 316T110
7G MC10141
6G 316T110
5G MC10141
ESYMCLK+
EPXCLK+
ESI+ P2-38
R26 470
R25 470
R7 470
SYMØ+ P2-28
SYM1+ P2-29
SYM2+ P2-30
SYM3+ P2-31
SYM4+ P2-32
SYM5+ P2-33
SYM6+ P2-34
SYM7+ P2-35
SYM8+ P2-36
SYM9+ P2-37
R18 330
P2-25 ALTCHSET-
2D 74LS04
ECURSOR-
EBLINK-
EREVID+
E(BLINK+
UNERLINE)+
P2-39 CVIDEO-
J13-7 AUX VIDEOB
J13-8 AUX VIDEOA
INTENSIFY+
P2-21 B2
J7-20
3G
MC10102 x4
2G MC10107
1G MC10105
RP7 470
RP8 470
RP9 470
RP6 470
RP5 470
TP7
TP8
J13-1
J13-3
J13-4
J13-6
HBVIDEO+ J7-16

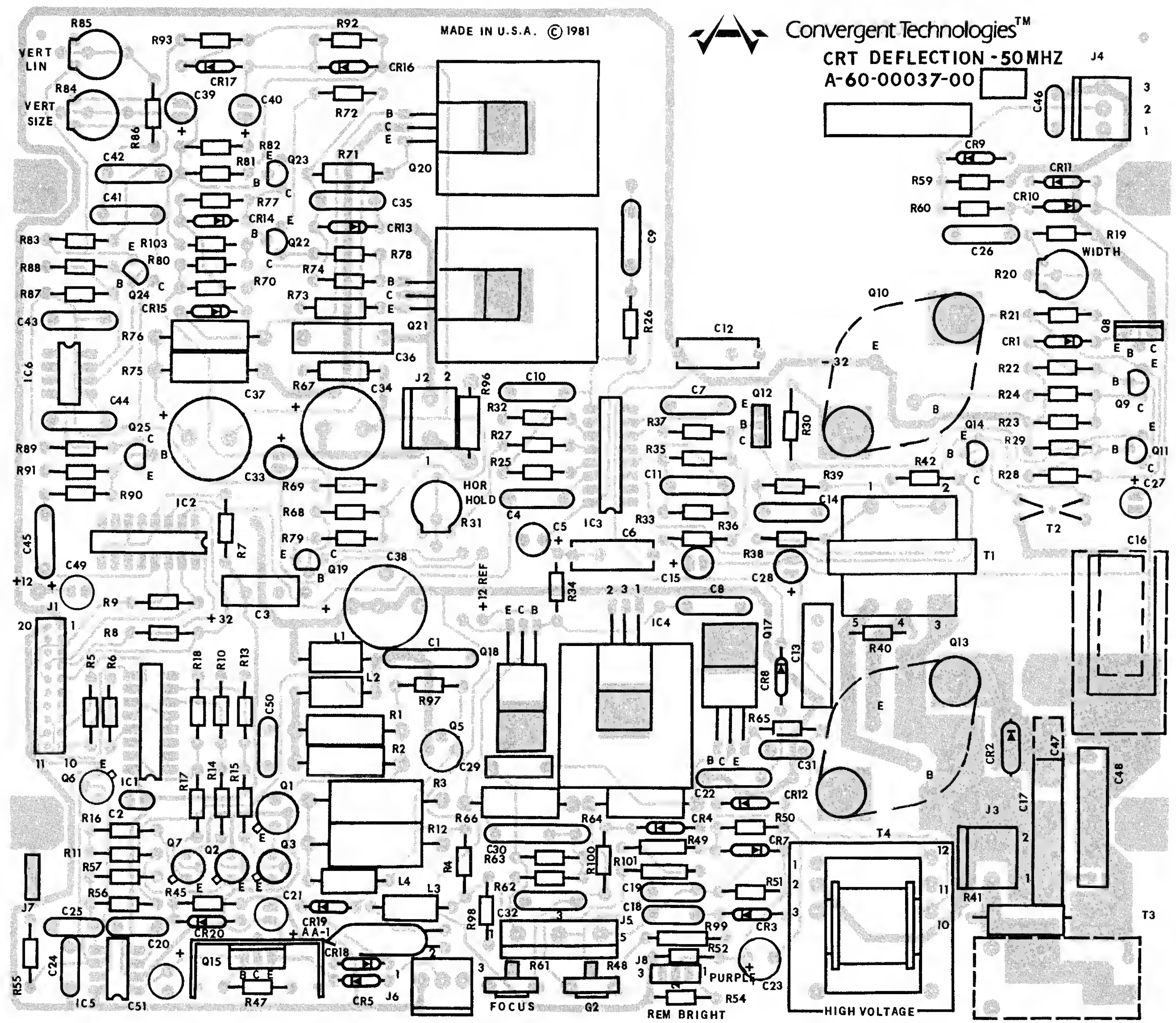

HFULL+
SELB -
ROWCLK-
SYMCLK-
PURIØ
15G
74LS74
DROWCLK-
CP+
NO ATTR+
15D
74LS74
PULL UP+
DATALD-
VIDACK+
VIDACK-
13D
74LS244
12C
74S04
OUT-
10C
74LS32
ACK-
MEMRD-
BLANK-
AUX+
EOP-
14D
74LS02
10B
74S74
LEOP+
MEMCLK+
11G
74LS244
RESET-
STOPDMA-
15A
6301
14A
6301
13A
6301
12A
6301
11A
6301
14B
74S374
12B
74S374
10A
74S374
13B
74S138
13C
74S139
14C
74S00
15C
74S151
15B
74S151
TP3
TP4
AUXWR-
11C
74LS139
AROWWR-
BROWWR-
AATTWR-
BATTWR-
ALATWR-
BLATWR-
LSN+
MSB-
LSB-
ADDRO-
LOADA-
INCR+
FULL+
OSYMWR-
ISYMWR-
CURSORWR-
STYLEWR-
WRENØ+
WREN1+
WREN2+
AUX-
VER BLANK+
GBLANK-
5B
74LS00
WAIT-
VIDACK+
VIDRQ+
11B
74S74
+5V
R1
1K
NO ATTR



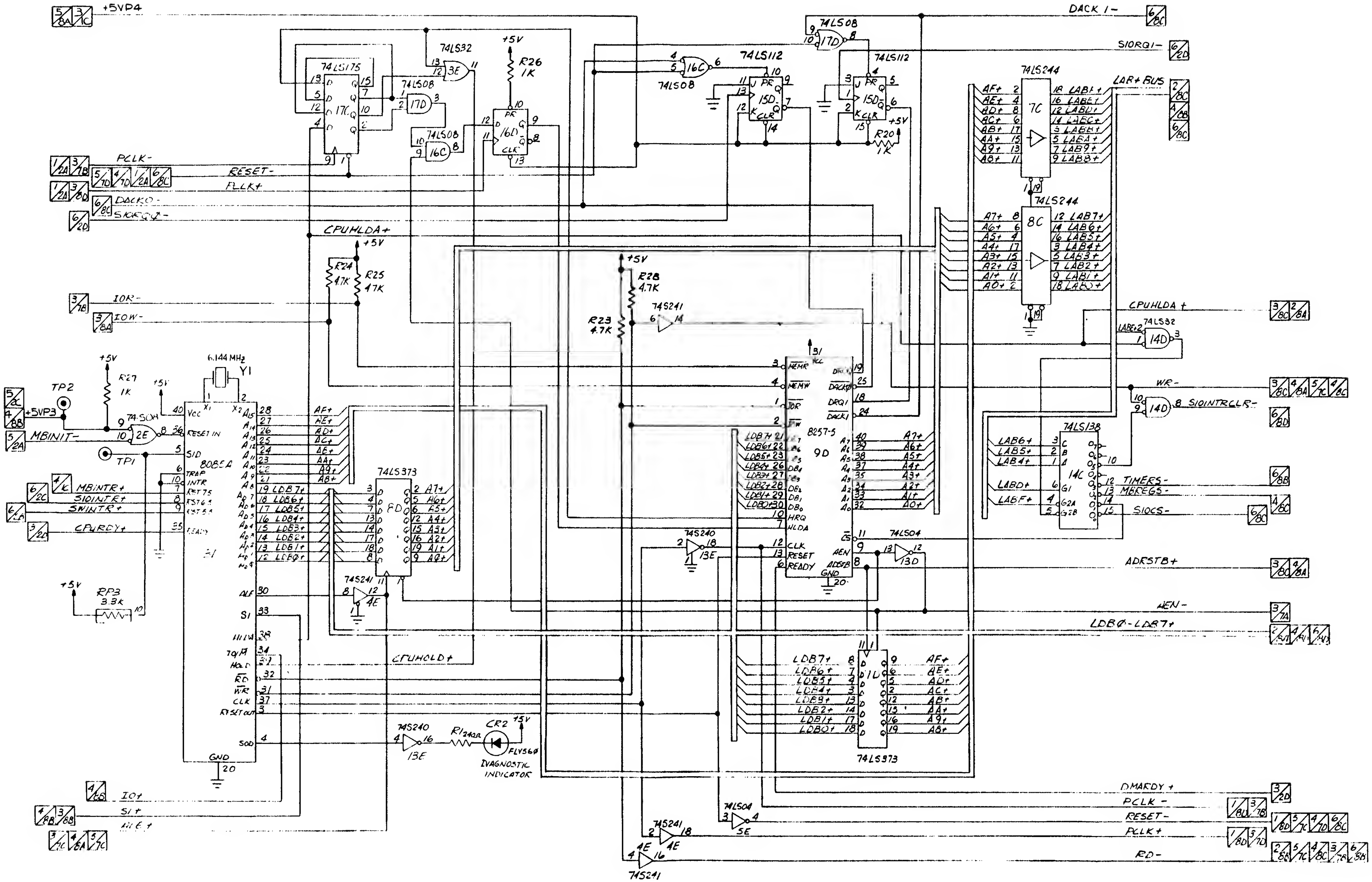
Video board (7 of 7)



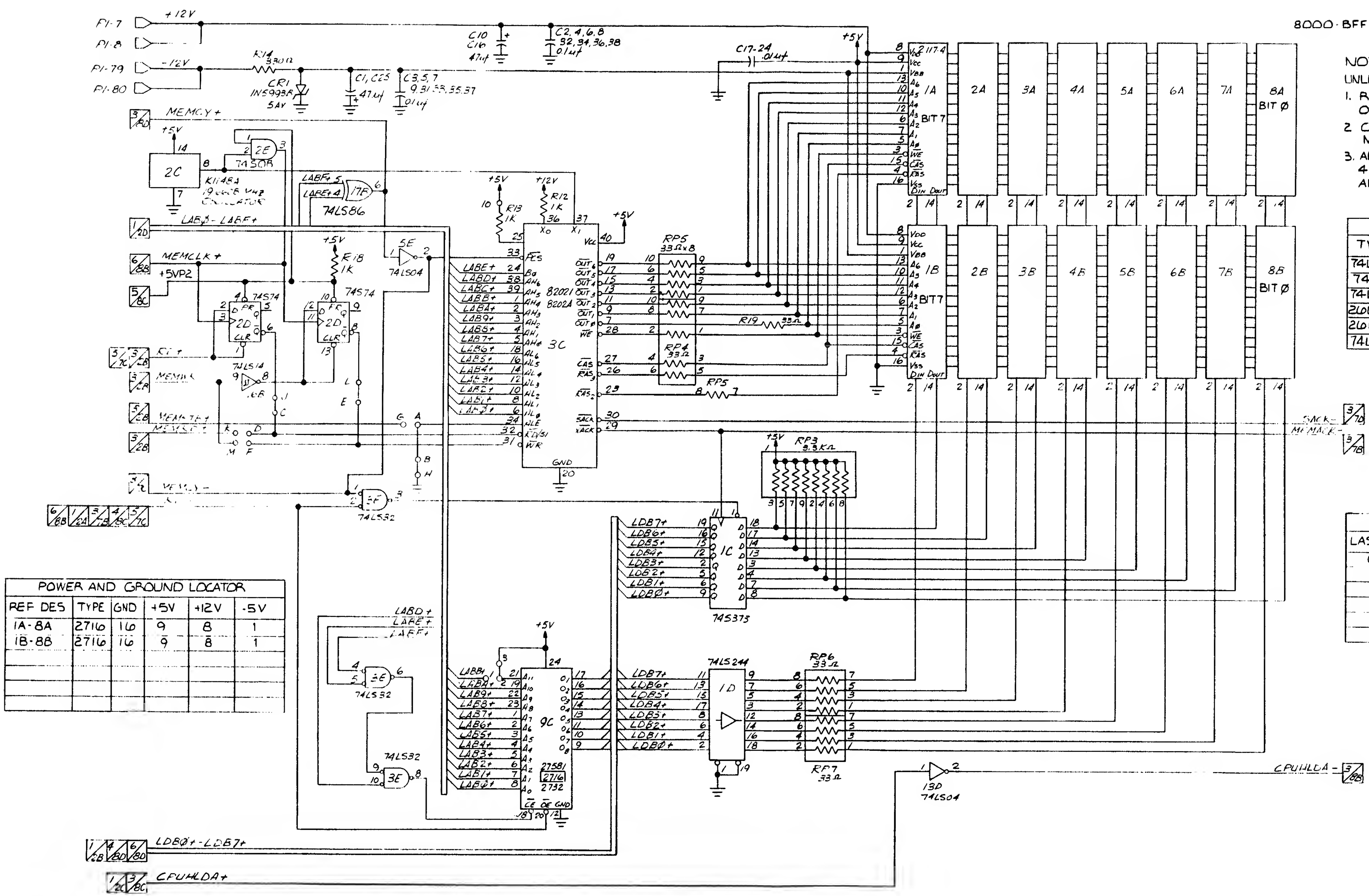
CRT Deflection System (schematic) (1 of 1)



CRT Deflection 50 MHz (assembly)   (1 of 1)



Comm I/O Processor board (1 of 6)



NOTES:

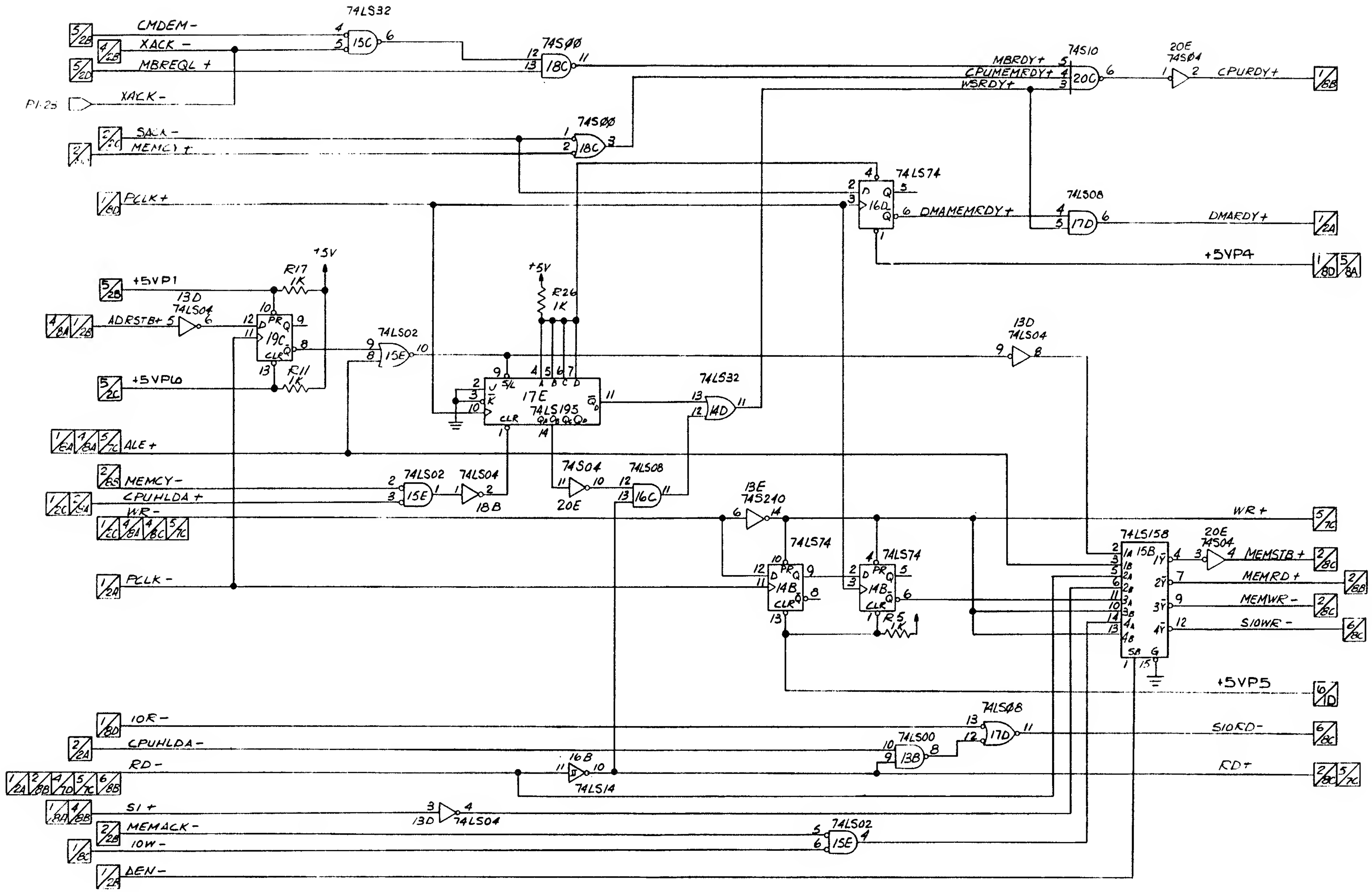
UNLESS OTHERWISE SPECIFIED:

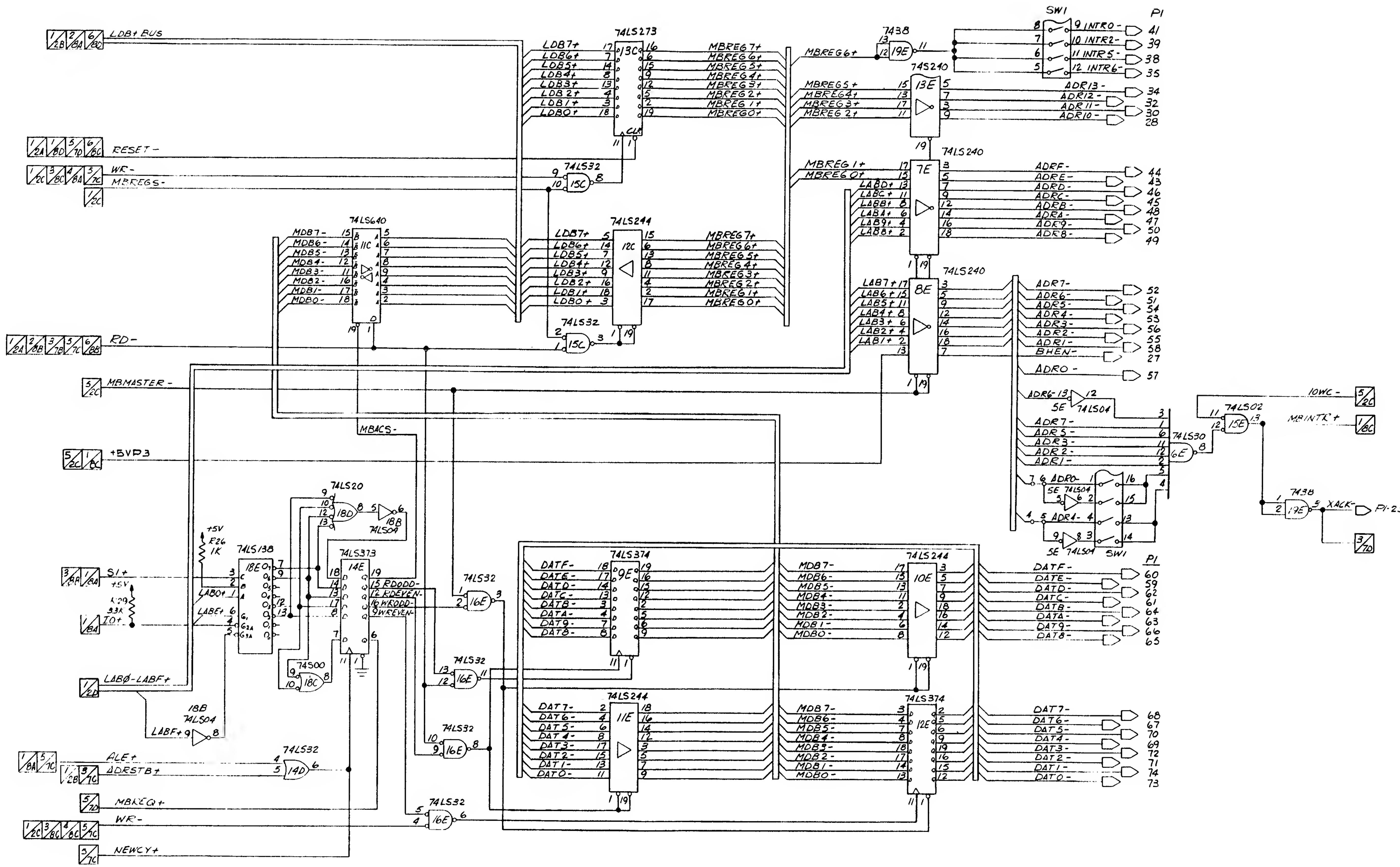
1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+6, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

SPARE GATES		
TYPE	REF. DESIGNATOR	QTY
74LS08	16C	1
74S10	20C	1
74LS14	16B	2
26LS31	15A	1
26LS31	17A	1
74LS112	20B	1

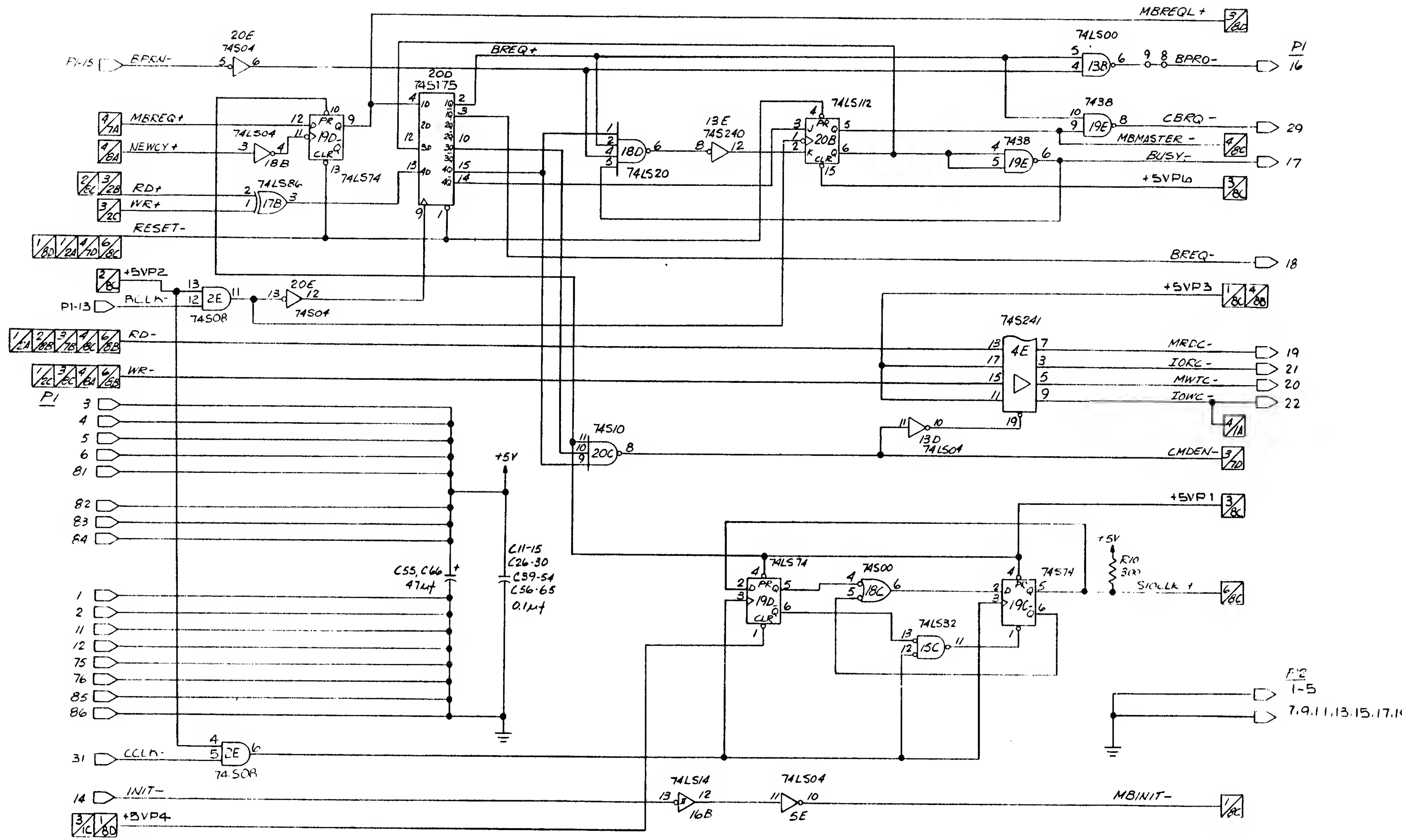
REF. DESIGNATORS	
LAST USED	NOT USED
CR2	
C66	
RP7	
R29	
SW2	
Y1	

POWER AND GROUND LOCATOR					
REF DES	TYPE	GND	+5V	+12V	-5V
1A-8A	2716	16	9	8	1
1B-8B	2716	16	9	8	1


CMDEM-
XACK -
MBREQL +
XACK-
SACK-
MEMCY+
PCLK+
+5VP1
ADRSTB+
+5VP6
ALE+
MEMCY-
CPUHLDA+
WR-
PCLK-
IOR-
CPUHLDA-
RD-
SI+
MEMACK-
IOW-
DEN-
MBRDY+
CPUMEMRDY+
WSRDY+
CPURDY+
DMAMEMRDY+
DMARDY+
+5VP4
WR+
MEMSTB+
MEMRD+
MEMWR-
SIOWR-
+5VP5
SIORD-
RD+
74LS32
74S00
74S10
74S04
74LS74
74LS08
74LS02
74LS04
74LS195
74S240
74LS158
74LS00
74LS14



Comm I/O Processor board (4 of 6)



Comm I/O Processor board (5 of 6)